2013 USENIX VAIL Computer Elements Workshop

June 23-26, 2013

Novel Computer Elements

Program Chair: Brian Hirano, Oracle, brian.hirano@oracle.com
Program Co-Chair: Steve Miller, NetApp, scm@netapp.com

Sunday June 23 5 PM Reception, Dinner and Keynote Presentation (**8:00 PM – 9:15 PM)**

Supercomputing the Universe

Key Note Speaker: Joel Primack, UCSC, joel@ucsc.edu Key Note Chair: Jim Hughes, jphughes@mac.com

Monday June 24

Session 1: Novel Processors — Chairs Yahya Sotoudeh, Intel & Pete Wilson
8:30 AM – 12:00 noon — yahya.sotoudeh@intel.com pete@kivadesigngroup.com
1.1 SeaMicro — Gary Lauterbach, AMD, gary.lauterbach@amd.com
1.2 Haswell Processesor — Rob Chappell, Intel, robert.s.chappell@intel.com
1.3 SPARC T5 — Rick Hetherington, Oracle, rick.hetherington@oracle.com
1.4 The Mill — Ivan Godard, ivan@ootbcomop.com

Session 2: **Security** — Chairs Mark Miller, Google & Dean Sutherland, CERT
1:00 PM – 4:30 PM — erights@google.com dsutherland@cert.org
2.1 Bitcoin — Brian Warner, warner@mozilla.com
2.2 Belay — Joe Politz, joe.politz@gmail.com
2.3 Tahoe-LAFS — Zooko Wilcox-O'Hearn, zooko@leastauthority.com
2.4 Thread Role Analysis for Secure Coding — Dean Sutherland, CERT, dsutherland@cert.org

Session 3: Embedded Asynchronous — Chairs Dave Baker, Firefly DSP & Marly Roncken, Portland State
8:00 PM – 10:15 PM — dave@fireflydsp.com marly.roncken@gmail.com
3.1 Multi-synchronous ICs — Ken Stevens, Granite Mountain Tech., kstevens@granitemountaintechnologies.com
3.2 Hurricane Damage Assessment — Alex Wegznek, UNF, g.wegznek@unf.edu
3.3 Asynchronous Chips for Forth Computers — Chuck Moore, GreenArrays, Inc., chipchuck@colorforth.com
3.4 Software Defined Networking — Jan Medved, Cisco, jmedved@cisco.com

Tuesday June 25

Session 4: Consumer Electronics — Chairs Atsushi Hasegawa, Renesas & Hirofumi Sumi, TSMC
8:30 AM – 12:00 noon — atsushi.hasegawa.gx@rms.renesas.com hsumi@tsmc.com
4.1 High-Speed Asynchronous Design — Makoto Ikeda, University of Tokyo, ikeda@silicon.u-tokyo.ac.jp
4.2 High-Speed vision and Manipulation — Akio Namiki, Chiba University, namiki@faculty.chiba-u.jp
4.3 Silicon Photonics and Applications — Koji Yamada, NTT Labs, yamada.koji@lab.ntt.co.jp
4.4 Augmented Service Process Reengineering — Takeshi Kurata, AIST, t.kurata@aist.go.jp

Planning Session: IEEE Vail 2014, 4PM – 5:30 PM All invited to participate.

Session 5: **Scale Out Architecture** — Chairs Michael McGrath & Don Banks, Cisco
8:00 PM – 10:15 PM — pawnmove@gmail.com donbanks@cisco.com
5.1 I/O Hinting — Mike Mesnier, Intel Research, michael.mesnier@intel.com
5.2 Implications of Next Generation Flash — Bill Moore, DSSD, bill@dssd.com
5.3 High Performance Scale Out Storage — Andy Warfield, Convergent.io, andy@convergent.io
5.4 Guaranteed QoS in the Cloud — Dave Wright, SolidFire, wrightd@gmail.com

Wednesday June 26

Session 6: Novel Materials — Jim Hughes, Seagate
8:30 AM – 12:00 noon — jphughes@mac.com
6.1 Hydrogen Depassivation Lithography — Josh Ballard, Zyvexlabs, jballard@zyvexlabs.com
6.2 Edison Returns! — Ron Vinsant, Exar, ron@poweracumen.com
6.3 Future of Tape — Richard Dee, Quantum, richarddee@comcast.net
6.**4 Future of Rotating Storage** — Tim Rausch, Seagate, tim.rausch@seagate.com

Committee

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