The following is the outline of sessions for the Vail 2005 workshop.

If you are interested in making a presentation, please contact the session chair.
For further information please contact:

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**Future Visions**

Program Chair: Allan Knies, Intel, allan.knies@intel.com
Program Co-Chair: Tom Conte, NC State University, conte@ncsu.edu

*Sunday, June 26 - Social hour followed by dinner & Keynote Presentation.*

**Intelligent DRAM - Challenges & Opportunities**
Speaker: Peter Hsu, Consultant, peterhsu@cs.wisc.edu
Keynote Chair: Bill Mangione-Smith, UCLA, billms@ucla.edu

*Monday, June 27*

**Session 1**
POWER & PACKAGING
Chair: Ray Barrett, Maxim, rlb@design.mxim.com
Chair: Bradley McCredie, IBM, mccredie@us.ibm.com
1.1 Thermal Design: Workstations & Servers, Andy Delano, HP
1.2 3D Packaging Trends, Bob Patti, Tezzaron
1.3 Military & Space Power, Jack McGirr, AKE
1.4 System Power & Cooling, Mike Nealon, IBM

**Session 2**
Panel: BEYOND MOORE'S LAW
Chair: Carl Anderson, IBM, cja@us.ibm.com
Chair: James Hughes, StorageTek, James_Hughes@storagetek.com

2.1 CMOS Technology Perspective, Emmanuel Crabbe, IBM

2.2 Design Perspectives, Stefan Rusu, Intel
2.3 Future Systems Perspective, Rich Oehler, AMD

2.4 LP CMOS via Probabilistic Computing, Krishna Palem, GA Inst. of Tech

Session 3
EMBEDDED PROCESSORS
Chair: Jim Slager, SuperH, jslager@iname.com
Chair: Tom Conte, NC State University, conte@ncsu.edu
3.1 New NAND Gate: Xtensa Processor, Bill Huffman, Tensilica
3.2 PowerPC Architectural Advancements, Pete Wilson, Freescale
3.3 3D Media Processor, Gerrit Slavenburg, NVIDIA

Tuesday, June 28

Session 4
CONSUMER ELECTRONICS
Chair: Michinori Nishihara, IBM, michi@jp.ibm.com
Chair: Yoshiaki Hagiwara, Sony, yoshiaki.hagiwara@jp.sony.com
4.1 10 Gbps Wireless Millimiter Waves, Takao Nagatsuma, NTT
4.2 Imager Sensor Technology, Hirofumi Sumi, Sony
4.3 Next Generation DVD Codec, Tetsuya Hara, Renesas Technology
4.4 Cell Processor Programming Features, Barry Minor, IBM

Session 5
PETAFLOPS SYSTEM TRADEOFFS PANEL
High Productivity Computing Systems
Chair: Alan Charlesworth, Sun, alan.charlesworth@sun.com
Chair: Robert Guernsey, IBM, guernsey@us.ibm.com
5.1 IBM HPCS Panelist, Balaram Sinharoy

5.2 Cray HPCS Panelist, Mike Parker
5.3 Sun HPCS Panelist, Brian O’Krafka
5.4 SGI HPCS Panelist, Steve Miller, SGI
5.5 IBM HPCS Panelist, Jeff Burns, IBM

Wednesday, June 29

Session 6
LOW POWER WIRELESS COMMUNICATIONS
Chair: Ed Callaway, Motorola, ed.callaway@motorola.com
Chair: Bob Montoye, IBM, montoye@us.ibm.com
6.1 LP Rad Tolerant CPU, Jody Gambles, U. of Idaho
6.2 LP via Scaling, Leland Chang, IBM
6.3 Energy Scavenging Technologies, Rajeevan Amirtharajah, UC Davis
6.4 Space Flight Telecommunications
  Chris Haskins & Wes Millard, Johns Hopkins Univ.

**Contacts**

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- Jerry Merckel, University of North Florida
- Jim Hughes, StorageTek
- Frank Mikalauskas, Hewlett-Packard
- John Polhemus, Consultant
- Ron Bell, Math Star
- Michinori Nishihara, IBM

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If you have any comments or suggestions regarding the Computer Elements web page, please send an e-mail to gmerckel@unf.edu.