

Program - Mesa 2000

2000 IEEE COMPUTER ELEMENTS MESA WORKSHOP

January 16-19, 2000

Workshop:

General Co chair: Robert Montoye, IBM Research (914) 945-3075

General Co chair: Wen-Hann Wang, Intel (503) 696-3048

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Workshop Theme: Low-Power Design Issues

Sunday Jan 16

5:00 Registration followed by Dinner and Keynote Presentation

Power Challenges in the Internet World

Stephen L. Smith

VP Intel Corporation

Monday Jan 17

Session 1. Low Power Design Contest Chair: Vivek Tiwari

1.1. A Low Energy Embedded FPGA

Varghese George, EECS Dept, University of California at Berkeley

1.2. A Variable Frequency Parallel I/O Interface with Adaptive Power Supply Regulation

Gu-Yeon Wei, Computer System Lab, Stanford University

1.3. 0.5V CMOS Logic Delivering 25 Million 16x16Bit Multiplications/s at 400fJ based on a 100nm T-gate SOI Technology

Dr. Reinhard Grube, Institut fuer Mikroelektronik Stuttgart (affiliated with the University of Stuttgart)

1.4. Low power self-timed divider with redundant signed digit representation Jae-Hee Won, Seoul National University

1.5. Designing a Low-Power DCS1800-GSM/DECT Modulator/Demodulator

Nikos D. Zervas, University of Patras, GREECE

1.6. Trends in Microarchitecture and Power Challenges

Prof. Trevor Mudge

1.7. Power Savings through Microarchitecture

Prof. Dirk Grunwald

Session 2. Consumer Appliances Chair Yoshiaki Hagiwara

2.1. CMOS Camera on a Chip

Eric Fossum, Photobit (60 min)

2.2. Overview and Market Trend of Digital Still Camera

Hirofumi Murase, Sony Corporation, Japan

2.3. Sony Digital Still Camera System Architecture, Product and Technical Features

Hirofumi Murase, Sony Corporation, Japan
2.4. sRGB vs. ICC; Color Management Scheme for Consumer Appliances
Naoya Kato, Sony Corporation, Japan
2.5. LSI chipsets behind Consumer Appliances
Yoshiaki Hagiwara, Sony, Japan

Session 3. Panel Discussion: Next steps in Low Power
Chair Deo Singh

Tuesday Jan 18

Session 4. Optical Devices Chair Michinori Nishihara

- 4.1. Photonic networks for the future network infrastructure
Ryo Matsunaga NTT
- 4.2. Advanced Optical Devices for Photonic Networks
Kenichi Kobayashi, NEC
- 4.3. Electromagnetic Bandgaps at Photonic and Radio Frequencies
Eli Yablonovitch, UCLA

Session 5. I/O Technology

- Cochairs Steve Hunter and John Alexander
- 5.1. Beyond PCI System I/O
Steve Hunter, IBM
 - 5.2. Software Engineering Tutorial
Neal Coulter, Univ. of North Florida
 - 5.3. Satellite RF
Frank van Diggelen, Magellan

Wednesday Jan 19 (Morning)

Session 6. Merged Logic Dram Chair Robert Montoye

- 6.1. Iram State and Future Plans
Joseph Gebis Berkeley
- 6.2. "eDRAM Technology Challenges"
Paul Parries
- 6.3. A New Approach for DRAM Function Partitioning by Waferscale Thin Layer Stacking
Robert Patti
- 6.4. Packaging alternatives to SOC with a hardware example
Robert Montoye

LOW POWER DESIGN CONTEST

Deadline Extended to October 1, 1999

Mesa, AZ; January 16-19, 2000

The IEEE Computer Elements Workshop is holding a Low Power Design Contest to provide a forum for universities and research organizations to showcase original "power-aware" designs and to highlight the innovations and design choices targeted at low power

The best designs will be selected and invited for presentation and exhibition at the workshop in Mesa, AZ, January 16-19, 2000. A special session in the workshop will be devoted to the Low Power Design Contest.

An industry-sponsored fellowship will be awarded to each selected design entry to defray the travel expenses for one speaker. The registration fee for the conference will also be waived for the speaker.

A call for submissions appears below. The deadline for submissions in **October 1th, 1999**. Entries can be submitted electronically (in PDF or Postscript format) or by sending 5 paper copies plus a

ATTN: Low Power Design Contest Chair

Vivek Tiwari

Intel Corp.

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Santa Clara, CA 95051

USA

Email: Vivek.Tiwari@intel.com

Low Power Design Contest Technical Committee

Prof. Anantha Chandrakasan, MIT

Prof. Massoud Pedram, USC

Prof. Takayasu Sakurai, Univ. of Tokyo, Japan

Prof. Christer Svensson, Linkoping Univ.

Prof. Francky Catthoor, IMEC, Belgium

Prof. Eby Friedman, Univ. of Rochester

Prof. Kaushik Roy, Purdue Univ.

Prof. Vojin G. Oklobdzija, UC Davis

Prof. Anshul Kumar, IIT Delhi, India

Prof. Sarma Vridhula, Univ. of Arizona

CONTEST SUBMISSIONS

- Submissions of *original designs (h/w or s/w)*, developed at universities and research organizations after January 1997 are invited.
 - Submissions should contain the title of the project, a 60-word abstract and a complete description of the design, not exceeding 4000 words in text.
 - The submission should clarify the originality, distinguishing features, and the measured performance metrics of the design.
 - The power targets for the design, the design choices related to power, and the specific optimizations, techniques and tradeoffs used to reduce power need to be highlighted.
 - Submissions which present proof-of-implementation in the form of die, board or system photographs and measurement data will be rated higher.
 - Submitted designs should not have received awards in other contests.
 - Submissions will be reviewed by a special committee of experts from academia and the industry.
 - Selected designs will be presented and exhibited at the workshop.
 - Each paper copy submission should include one cover page and five (5) stapled copies of the complete manuscript. The one cover page should include:
 - 1. Name, affiliation and address of each author
 - 2. A designated contact person, including his/her telephone number, fax number, and email address
 - 3. A designated presenter, should the paper be accepted
 - 4. The following signed statement:
 - " All appropriate organizational approvals for the publication of this paper have been obtained. If accepted the author(s) will select a designates speaker to present the paper at the Workshop"
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If you have any comments or suggestions regarding the Computer Elements web page, please send an e-mail to:
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