

2016 USENIX

VAIL Computer Elements Workshop

June 19 - June 22, 2016

Program Chair: David Flynn, ARM, david.flynn@arm.com
Program Co Chair: Steve Miller, Intel, steven.c.miller@intel.com

Sunday June 19, 5 PM Registration, Dinner and Keynote Presentation

Cryptography in the New World Order

John Kelsey, NIST

Key Note Chair: Jim Hughes, jphughes@mac.com

Monday June 20

9:00 AM – 12:00 noon

Session 1: Processors

Chairs: Jay, Fleischman, AMD, Jay.Fleischman@amd.com
Richard Grisenthwaite, ARM, richard.Grisenthwaite@arm.com

- Intel Quark Processor
- RISC-V: Instruction sets want to be free
- X-Gene3

Venkat Madduri, Intel, venkateswara.madduri@intel.com
Krste Asanovic, UC Berkeley, krste@berkeley.edu
Greg Favor, AppliedMicro, gfavor@apm.com

1:30 PM – 4:30 PM

Session 2: Consumer

Chairs: Atsushi Hasegawa, Renesas, atsushi.hasegawa.gx@renesas.com
Yoshio Masubuchi, Toshiba, yoshio.masubuchi@toshiba.co.jp

- Normally-Off Computing
- Microcontroller for Small Sensing Nodes
- LIDAR for ADAS and autonomous vehicles
- Automotive Lidar technologies

Hiroshi Nakamura, Univ Tokyo, nakamura@hal.ipc.i.u-tokyo.ac.jp
Masami Nakajima, Renesas, masami.nakajima.wj@renesas.com
Ken Tanabe, Toshiba, kenn.tanabe@toshiba.co.jp
Harvey Weinberg, Analog Devices, harvey.weinberg@analog.com

Tuesday June 21

9:00 AM – 12:00 noon

Session 4: OS and Security

Chairs: Michael Aien, Analog Devices, michael.aien@analog.com
Steve Miller, Intel, steven.c.miller@intel.com

- Barrelfish: an operating system for modern hardware
- SeaOS: A simple OS for multicore Machines
- Haven: Shielding Applications from an Untrusted Cloud
- Failure Provenance Analysis: From Crashdump to Shellcode

Timothy Roscoe, ETH, troscoe@inf.ethz.ch
Daniel Bittman, UCSC, danielbittman1@gmail.com
Andrew Baumann, Microsoft, Andrew.Baumann@microsoft.com
Parker Thompson, Leviathan, Parker.Thompson@leviathansecurity.com
Baron Von Oldenberg, Baron.Oldenburg@leviathansecurity.com

Planning Session: VCEW 2017, 4PM – 5:30 PM All invited to participate.

8:30 PM – 10:00 PM

Session 5: Internet of Things

Chairs: Pete Wilson, NXP, peter.wilson@nxp.com
Bill Huffman, Cadence (Tensilica), huffman@alum.mit.edu

- IoT: The Next Technology Cycle
- Bringing Deep Learning to the Mass Market

Krisztian, Flautner, ARM, Krisztian.Flautner@arm.com
Samer Hijazim, Cadence, shijazi@cadence.com

Wednesday June 22

9:00 AM – 12:00 noon

Session 6: Process and GPU

Chairs: Yahya Sotoudeh, Intel, yahya.sotoudeh@intel.com
David Flynn, ARM, david.flynn@arm.com

- Low Voltage SRAM
- Accelerating Hyper Cloud Data Center Solutions with Breakthrough Integration Technologies
- The Bifrost GPU architecture and the ARM Mali-G71 GPU

David Burnett, Global Foundries, david.burnett@globalfoundries.com
Sanjay Charagulla, Global Foundries, sanjay.charagulla@globalfoundries.com
Jem Davies, ARM, Jem.Davies@arm.com

VCEW Support Corp: John M. Polhemous
jpbookworm23@gmail.com
Committee Chair: Jim Hughes
jphughes@mac.com

Registration Chair: Jim Hughes
jphughes@mac.com
Comm. Vice Chair: Steve Miller
steven.c.miller@intel.com

Finance Chair:
TBD
Asia Pacific Chair: Atsushi Hasegawa
hasegawa.atsushi@renesas.com