The Vail Computer Elements Workshop

The Complete Program Collection

From 1996 to the present

Program - Vail 1996

1996 IEEE

Computer Elements Vail Workshop

Vail, Colorado
June 23-26, 1996
Workshop Theme: Back to the Future

Sponsored by the IEEE Computer Society's
Technical Committee (TC) on Computer Elements

Sunday, June 23, 1996

Evening Keynote Address: Microprocessor Outlook: 1997-2000"
Michael Slater, MicroDesign Resources.
Session Details

Monday, June 24, 1996

Session One: Mass Storage Technology and I/O Subsystems(8:30am)
Session Chair: Bob Montoye, IBM Almaden Research Center, San Jose, CA
Co-chair: Jeff Connell, Amdahl Corp., Sunnyvale, CA
1 .a. "Disk Drive Technology: The Next 50 Years",
Speaker: Currie Munce; IBM Almaden Research Center, San Jose, CA.
1 .b. "Holographic Storage",
Speaker: Geoffrey Burr; IBM Almaden Research Center, San Jose, CA.
1 .c. "Gigabit Ethernet",
Speaker: Howard Johnson; Olympic Technology Group
1 .d. "Fibre Channel Mass Storage",
Speaker: Richard Taborek; Amdahl Corp., Sunnyvale, CA.
Session Two: Systems on a Chip: Large ASIC Design (1:30pm)
Session Chair: Laszlo Gal, Motorola, Austin, TX. (Calvin Harrison acting)
2.a. "Design Challenges for One-Million-Gate ASICs"
Speaker: Mike Trick; IBM Microelectronics, Essex Junction, VT.
2.b. "System on a Million Gate Chip: Design Tools for Fast Turn-Around"
Speaker: Merrill Hunt; Cadence Design Systems, San Diego, CA.
2.c. "Million Transistor Mixed-Signal Designs"
Speaker: Dave Baker; Brooktree Corp., San Diego, CA.
2.d. "Hardware/Software Co-Design of Systems on a Chip"
Speaker: Calvin Harrison; Motorola, Austin, TX.
Session Three: Display Technology I Panel Session (8:00pm)
3.a "LCD Displays"
Speaker: Zenzo Tajima, Hitachi Ltd., Tokyo, Japan.
Panel Session: Open Microphone

Tuesday, June 25, 1996

Session Four: SMP and Cluster Systems & Interconnects (8:30am)
Session Chair: Cheng Kong; Tandem Computers, Cupertino, CA.
Co-Chair: Joel Boney, HaL Computer Systems, Campbell, CA.
4.a. "Issues and Non-Issues in the Design of Clusters"
Speaker: Greg Pfister; IBM Corp., Austin, TX.
4.b. "How to Break Bus/Backplane Bottlenecks for SMP Without
Breaking the Bank"
Speaker: Wolf Weber; HaL Computer Systems, Campbell, CA.
4.c. "Remote Distributed Memory on Clustered NT Workstations:
NT Clusters on ServerNet",
Speaker: Gary Campbell; Tandem Computers, Cupertino, CA.
4.d. "Building a General Purpose Multi-computer: The Solaris MC Approach",
Speaker: Madhusudhan Talluri; Sun Labs, Mountain View, CA.

Afternoon free for technical interchange

Session Five: High Perf. Circuits & Clock Distribution (8:00pm)
Session Chair: Carl Anderson; IBM Research, Yorktown Heights, NY.
Co-Chair: John Stahler; IDT Corp., Santa Clara, CA.
5.a. "CMOS Circuit Design Challenges for High Speed Microprocessors"
Speaker: David Greenhill, Sun Microelectronics; Sunnyvale, CA.
5.b. "L, R and C in High Speed Clock and Signal Lines",
Speaker: Phil Restle; IBM Research, Yorktown Heights, NY.
5.c. "Tradeoffs in High Speed Microprocessor Circuit Design",
Speaker: Sam Naffziger; Hewlett Packard Co., Fort Collins, CO.

Wednesday. June 26.1996

Session Six: The PC: Today and Tomorrow (8:30am)
Session Chair: Jim Slager; Hitachi Micro Systems, Inc.; San Jose, CA.
Session Co-Chair: Richard Crisp; Rambus Inc., Mountain View, CA.
6.a. "The Changing PC Landscape"
Speaker: Michael Slater; MicroDesign Resources, Sebastopol, CA.
6.b. "The Business and Technology Trends that Will Shape PC2OOO"
Speaker: Fred J. Pollack; Intel Corp., Hillsboro, OR.
6.c. "PC Manufacturing"
Speaker: Sheau-Jiung Lee, Acer Labs, San Jose, CA.
6.d. "Meeting PC Multimedia Needs with the Media Processor"
Speaker: Pete Foley; Chromatic Research, Sunnyvale, CA
Workshop Ends Wednesday June 28, 1:00pm

Program - Europe 1997

IEEE Computer Elements Technical Committee

1997 IEEE Computer Elements European Workshop

Portofino, Italy

March 23-26, 1997

Committee Chair and General Chair: Douglas Westcott, IBM (914)435-8652
General Co-chair: Mario Vinsani, Bull 39-2-6779-8244
Arrangements/Registration: Luisa Cassaro, Bull 39-2-6779-8465
Finance Chair: Mario Vinsani, Bull
For Information, contact: Luisa Cassaro 39-2-6779-8465

Workshop Theme: THE CHANGING EUROPEAN ELECTRONICS LANDSCAPE

Sunday, March 23, 1997

Keynote Address: Pen Based Computers or Computer Based Pens?
What is the right paradigm for the future of electronics?
Alberto Sangiovanni Vincentelli, Univ. Berkeley

Monday, March 24, 1997

Session I: Round Table on Electronics Evolution, Impact on the Electronics Industries and the European Society.
Round Table Chair: Roberto Del Moretto, European Commission

Participants: Maurizio Decina, CEFRIEL
Bernado Del Monego, IBM Italy
Pierre Ensch, Magneti Marelli
Heikki Huomo, Nokia
Bill Lattin, Synopsys
Robert Lech, Cadence
Ennnio Ponzetto, Olivetti
Bruno Ricco, Bolgna University
Alberto Sangiovanni Vincentelli, Univ. Berkeley
Enrico Villa, SGS Thomson
Mario Vinsani, European Chair IEEE Computer Elements
Douglas Westcott, Chair IEEE Computer Elememts
Advance Research Projects and ESPRIT Programs- Framework IV-V
Roberto Del Moretto, European Commission-Directorate III

Session II: Computers, Web Computers and Multimedia Systems

Session chair: J. Talbot, Bull

II.1 Open System evolution
Jacques Talbot, Bull
II.2 Design of the Family of IBM Network Computers
Al Talkington, IBM Austin
II.3 Role of Smart Cards for the Internet
Pierre Parasdinas, GEMPLUS - Gemenon Cedex
II.4 Java and Internet Applications
Francesco Iarlori, SUN Microsystem-Italia
II.5 Internet over Direct Broadcasting Satallite
Horst Clausen, University of Salisburg

Session III: Communication Systems and Wireless Systems

Session chair: Heikki Huomo, Nokia

III.1 Integrated GPS and Wireless Communication Technologies
William Dussell, Trimble Navigation
III.2 Wireless System: Today and Tomorrow
Heikki Huomo, Nokia
III.3 Maritime Navigation System

G. Carnivali, Navionics

Tuesday, March 25, 1997
Session IV: New Design Methodologies and New CAD Tools
Session chair: Prof. Alberto Sangiovanni Vincentelli, Berkeley
and Rome Universities.

IV.1 New Paradigms for System Design
Prof. Alberto Sangiovanni Vincentelli, Berkeley and Rome Universities
IV.2 Hardware and Software Codesign
Karl Van Rompaey, CoWare
IV.3 Design Reuse Challenge
Bill Lattin, Synopsys

Session V: The New Embedded Processors
Session Chair: Robert Krysiak, SGS Thompson

V.1 Embedded Processor-The Challeneg of Superintegration
Robert Krysiak, SGS Thomson
V.2 Trends in High Volume Embedded Proceesors
Tudor Brown, ARM
V.3 Hyperstone, A Small Low Power, Low Cost Macro cell
Manfred Schlett, Hyperstone
V.4 PowerPC Embedded Processor
Elliot Newcombe, IBM

Informal Technical Exchange
Planning Meeting for those interested

Wednesday, March 26, 1997
Session VI: Electronics in the Car
Session Chair: Pierre Ensch, Magneti Marelli

VI.1 Introduction
Pierre Ensch, Magneti Marelli
VI.2 Vehicle microelectronics - Technical status and future developments
H. Cuntz, Bosch
VI.3 Road telematic or interactivity between vehicle and infrastructure
D. Augello, Renault
VI.4 New structure in automotive electronics and their implications for development procedures and the collaboration between development partners. History, experience, and benefits.
C. Braklo, Mercedes
VI.5 From Car Stereo to Info Center and onward to a Multimedia
Distributed Architecture
P. Gonnella, SGS Thomson

12:15 End of Workshop

Program - Vail 1997

1997 IEEE

Computer Elements Vail Workshop

Vail, Colorado

June 22-25, 1997

Workshop Theme: "Technology Moves Too Fast To Worry About Themes!"

Sunday, June 22, 1997

Evening Keynote Address: "The Road to Microprocessor Autonomy"
Mike Johnson, Advanced Micro Devices.
Session Details

Monday, June 23, 1997

Session One: Cryptography and Security in Internet Commerce (8:30 am)
Session Chair: Bill Worley, Hewlett Packard Company.
Co-chair: Herb Schorr, USCIISI

I.a. "The State Of The Art Of Encryption",
Speaker: Jeff Schiller, Massachusetts Institute of Technology, Cambridge, MA
1.b. "Encryption At Hewlett Packard"
Speaker: Joe Pato, Hewlett Packard Company, Cupertino, CA.
1.c. "Encryption at IBM",
Speaker: Hamid Ahmadi, IBM Watson Research Lab, Hawthorne, NY.
1.d. "Encryption at Microsoft"
Speaker: George Spix, Microsoft Corp., Redomd, WA.
Session Two: New ISA's (DSP and MMX) (1:30 pm)
Session Chair: Ron Bell, LSItogic
Co-Chair: Jeff Yetter, Hewlett Packard Company
2.a. "CDSP"
Speaker: Peter Koeppen, Texas Instruments
2.b. "Extending Existing Architectures to Optimize Stream Processing"
Speaker: James Wei, Fusion Micro Media
2.c. "What does MMX(tm) mean?"
Speaker: Larry Mennemeier, Intel Corporation.
2.d. "Do instruction sets matter anymore?"
Speaker: Ron Bell, LSI Logic
Session Three: Open Mic Session (8:00 pm)
Session Chair: Greg Blanck
"Open Mic" presentation & discussion of timely subjects.
Session Four: IC Technology and Embedded Memories (8:30 am)
Session Chair: Carl Anderson, IBM
Session Co-Chair: Hirohsi Yoshimura, NTT
4.a. "The Future of CMOS Technology"
Speaker: Ian Young, Intel Fellow, Intel Corp.
4.b. "High Speed Silicon Germanium Bipolar and BiCMOS Technology"
Speaker: Seshadri Subbanna, IBM East Fishkill
4.c. "The Limits of CMOS"
Speaker: Lewis M. Terman, IBM Watson Research Center
4.d. "DRAM Embedded Logic Overview - Potential and Future Applications"
Speaker: Hikaru Hida, NEC Corp.
4.e. "Impact of CMOS/S IMOX on low-power high speed LSIs"
Speaker: Yusuke Ohtomo, NTT
Session Five: Next Generation Microprocessors (8:00 pm)
Session Chair: Jim Slager, Hitachi

5.a. "IBM S/390"
Speaker: Charles Webb, IBM.
5.b. "HP PA8500"
Speaker: Jay Fleischmann, Hewlett Packard.
5.c. "DEC Alpha 21264",
Speaker: Dan Leibholz, DEC.
5.d. "Intel Mobile Microprocessors"
Speaker: Chip Krauskopf, Intel.

Wednesday, June 25, 1997

Session Six: DVD Applications (8:30 am)
Session Chair: Greg Blanck, Axil Computers
Co-Chair: Yoshiaki Hagiwara, Sony

6.a. "DVD Technology Trends"
Speaker: Mr.Takao Ihashi, Sony Corporation, Tokyo, Japan.
6.b. "Software and Hardware DVD Solutions"
Speaker: George Haber; Zoran CorporationlCompcore, Santa Clara, CA.
6.c. "DVD Drive Technology"
Speaker: Hiroharu Satoh, Toshiba.
Workshop Ends Wednesday June 25, 1:00pm

Program - Vail 1998

1998 IEEE Computer Elements Vail Workshop

Vail, Colorado

June 21-24, 1998

Sponsored by the IEEE Computer Society's: Technical Committee (TC)

on Computer Elements:

TC Chair: Douglas Westcott, IBM (914) 435-8652
Vice Chair (Vail) Jeff Yetter, Hewlett Packard Company (303) 229-3249
Japan Chair: Michinori Nishihara, IBM Japan 81-0775-87-6110
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John Polhemus (303) 781-6190
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Vail Workshop:

General Chair: Jeff Yetter, Hewlett Packard Company (970) 229-3249
Co-Program Chair Joel Boney, HP (970) 229-6518
Co-Program Chair Bob Guernsey, IBM (914) 435-8058
Arrangements: Ron Bell, Equator Technologies (408) 369-5477
Registration: John Polhemus, Consultant (303) 781-6190
Treasurer: John Polhemus, Consultant (303) 781-6190

Sunday Evening:

Keynote: The Next Decade of Moore's Law
Dr. Rick Baum, IBM Server Chief Architect

Monday Morning:

Announcements:
Yetter, Boney, Guernsey, Polhemus
Session 1. New ISA Processors
Chair: Jim Slager
Speakers:
A. "Sun MicroJava 701 CPU Core"
Speaker: Shailender Chaudhry, Sun Microsystems
B. "Philips Trimedia",
Speaker: Gert Slavenburg, Philips
C. "IRAM"
Speaker: Christoforos Kozyrakis, UC Berkeley
D. "Intel Merced",
Speaker: Michael Slater, Micro Design Resources

Monday Afternoon:

Session 2. Modern Server Technology
Chair: Gene Emerson Co-chair: John Norris
A. "Future High Performance Servers: The Balanced Solution",
Speaker: Charlie Johnson, IBM GigaProcessor project.
B. "Starfire:Extending the SMP Envelope,"
Speaker: Alan Charlesworth, Sun
C. "The HP V-Class: Developing a Successful Technical and Commercial Server,"
Speaker: Rich Adkisson, Hewlett Packard.
D. "Synfinity Interconnect for Highly Scalable Servers"
Speaker: David Rich, HAL Computer

Monday Evening:

Session 3. Silicon Technology, Cooling, Packaging

Chair: Carl Anderson Co-chair: Hiroshi Yoshimura
A. "PC Microprocessor Packaging and Cooling"
Speaker: Dennis Herrell, AMD
B. "Past, Present and Future of CCD Image Sensors"
Speaker: Sumio Terakawa, Matsushita
C. "Developement Strategy of SuperH Microprocessors for Multimedia Applications"
Speaker: Hideo Maejima, Hitachi Ltd.

Tuesday morning:

Session 4. Consumer Computing, PC and/or TV
Chair: Yoshiaki Hagiwara
A. "The Home of Tomorrow, Communications, Computing and Consumer"
Speaker: Peter Hortensius, IBM
B. "PC Audio for Consumer Computing"
Speaker: Wayne Galella, Cirrus Logic
C. "Web TV System Architecure and Technology"
Speaker: Tim Bucher, WebTV.
D. "Toshiba TV PC and Sony VAIO"
Speakers: Mikhail Tsinberg, IT Div. of Toshiba America
Isao Murase, Sony.

Tuesday evening:

Session 5. Internet, Security and Java
Chair: Jerry Merckel Co-chair: Bob Guernsey
A. "Internet Telephony"
Speaker: Keith Kelley, Netspeak
B. "e-Business Challenges with Java",
Speaker: Rob Smith, IBM
C. "Gator PC" (Java PC)
Speaker: John Alexander, Gator PC

Wednesday morning:

Session 6. Evolving I/O Technology
Chair: Bob Montoye Co-chair: Winfried Wilcke
A. "The Virtual Retinal Display: Toward the Ultimate Visual Interface",
Speaker: Tom Furness, Univ. of Washington
B. "Pen Input in Computing - An Overview",
Speaker: Krishna S. Nathan, IBM Watson Research.
C. "Deconstructiong Computers with 1394"
Speaker: Gary Hoffman, Consultant
D. "The Equator System on Silicon"
Speaker: David Baker, Equator

Program - Vail 1999

1999 Vail Computer Elements Workshop

June 27th – 30th 1999, Vail Colorado

Sponsored by the IEEE Computer Society's Technical Committee (TC) on Computer Elements
TC Chair: Douglas Wescott, IBM 914-435-8652
Vice Chair Jeff Yetter, Hewlett Packard 970-898-3249
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Vail Workshop:
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Program Chair Joel Boney, Hewlett Packard 970-898-6518
Arrangements Ron Bell, Micro Linear 408-369-5477
Registration John Polhemus, Consultant 303-781-6190
Treasure John Polhemus, Consultant 303-781-6190

Sunday Evening, June 27th:

4:00pm: Technical Committee Meeting. All Welcome
5:00pm: Social Hour Followed by Dinner
8:00pm: Evening Keynote Address: Microprocessors: Current and Future Trends
Speaker: Keith Diefendorff, Micro Design Resources

Monday, June 28th:

Session 1: Large Web and Commercial Servers
Session Chairs: John Norris, Bob Guernsey

1a. Title: *HP N Class Commercial Server*
Speaker: Bill Bryg, HP
1b. Title: *Fault Tolerance and Data Integrity in Non Stop Himalaya Computer Systems*
Speaker: Bob Jardine, Compaq
1c. Title: *Ultra-Sparc III Based Mid and High End Servers*
Speaker: Alan Charlesworth, Sun Microsystems
1d. Title: *Large Web Site Architecture*
Speaker: Jay Casler, IBM

Session 2: IA-64 Architecture Details
Session Chair: Dave Fotland, Co-chair: Joel Boney

2a. Title: *Instruction Repertoire, Functional Units, and Dispersal*
Speaker: David Fotland, HP
2b. Title: *Architectural Enhancements for high ILP*
Speaker: Allan Knies, Intel
2c. Title: *IA-64 Register Model: Stack & Rotation*
Speaker: Dale Morris, HP
2d. Title: *Compiling for IA-64*
Speaker: Carol Thompson, HP

Session 3: Low Power and Consumer Electronics
Session Chair: Nishihara-san, Co-chair: Senta-san,

3a. Title: *MTCMOS / SIMOX Technology: Potential and Future Applications*
Speaker: Yuichi Kado, NTT
3b. Title: *Sony Playstation 2 , Motivation, Requirements and Architecture Definition*
Speaker: Hidetaka Magoshi, Sony Computer Entertainment
3c. Title: *Sony Playstation 2, Implementation Technology for Emotion Engine*
Speaker: Mitsuo Saito, Toshiba

Tuesday, June 29th:

Session 4: IA-32

Session Chairs: Jim Slager, Bob Montoye.

4a. Title: *Pentium III with SSE*
Speaker: Shreekant (Ticky) Thakkar, Intel
4b. Title: *AMD K7*
Speaker: Jay Pickett, AMD
4c. Title: *Centaur WinChip*
Speaker: Dave Witt, Centaur
4d. Title: *IA-32 Summary*

Speaker: Keith Diefendorff, Micro Design Resources

Session 5: Microprocessors, Complex Chips, Systems on a Chip and Embedded DRAM

Session Chairs: Nishihara-san, Jay Fleischman,

5a. Title: *Macro Design, Architecture, Test and Application of Embedded DRAM*
Speaker: John Barth Jr., IBM
5b. Title: *Perspective on SSI and Impact on Memory*
Speaker: Richard Mattick, IBM
5c. Title: *Server Oriented Microprocessor Optimizations*
Speaker: Chuck Moore, IBM
5d. Title: *The Changing Landscape of System-on-a-Chip Design*
Speaker: Bill Lee, IBM

Wednesday, June 30th:

Session 6: eCommerce

Session Chairs: Bill Worley, Herb Schorr

6a. Title: *B2B and B2C Value Networks*
Speaker: George Spix, Microsoft
6b. Title: *Next Generation eCommerce Applications*
Speaker: Pedro Szekely, ISI
6c. Title: *eCommerce at HP*
Speaker: Joe Pato, HP
6d. Title: *Advanced Encryption Standards*
Speaker: Bill Worley, HP
Last updated: 6/17/99 10:55 AM

The 2000 Vail Computer Elements

Vail, Colorado

June 25-28, 2000

Sponsored by

IEEE Computer Society

The following is the outline of sessions for the Vail workshop as of May 5, 2000. Invitation letter follows session information. Click here for registration form.

For further information please contact:

Jerry Merckel
Phone: (904) 620-1350
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Sunday Afternoon / Evening, June 25

4:00pm - 5:00pm - Technical Committee Meeting in Sarah's Lounge (all welcome)
5:00pm - Social Hour Followed by Dinner
8:00 pm - Evening Keynote Address: Bob Guernsey, IBM

Monday, June 26

8:15 am - 8:30 am - Announcements and Introductions

8:30 am - 12:00 noon
Session 1 - High End Microprocessors
Chair: Jim Slager

1a. Title: *Intel Itanium.* Speaker: Hans Mulder, Intel
1b. Title: *IBM Power 4.* Speaker: Jim Kahle, IBM
1c. Title: *AMD Athlon.* Speaker: Jay Picket, AMD
1d. Title: *Intel Willamette.* Speaker: Dave Sager, Intel

1:00 pm - 4:30 pm
Session 2: On-chip Noise and Limits of CMOS
Session Chair: Carl Anderson

2a. Title: *Noise in CMOS VLSI Chips.* Speaker: Ken Shepard, Columbia University
2b. Title: *Noise, Package and Performance Considerations in Elastic I/O Design.* Speaker: Dan Dreps, IBM
2c. Title: *IBM Future CMOS Technology for ASICS and Microprocessors.* Speaker: Clement Wan, IBM
2d. Title: *JAZiO High Speed Interconnect.* Speaker: Jim Slager, *JAZiO*
2e. Title: *Future CMOS Technology.* Speaker: Tahir Ghani, Intel

8:00 pm - 10:00 pm
Session 3: Servers, High End CMOS Machines and RAS
Session Chairs: Linton Ward, Alan Charlesworth

3a. Title: *InfiniBand IO Architecture.* Speaker: Renato Recio
3b. Title: *S/390 System Architecture Directions.* Speaker: Guru Rao, IBM
3c. Title: *Compaq Wildfire.* Speaker: David Fenwick

Tuesday, June 27

8:15 - 8:30 - Announcements

8:30 am - 12:00 noon

Session 4: Networks, Communications, and Security

Session Chairs: David Baker, Jack Bigham

4a. Title: *Utilizing Unlimited Bandwidth for Global Collaboration.* Speaker: Mike Mott , Boeing

4b. Title: *Persistent Information Security and its Effects on Networking.* Speaker: Jim Hughes, Storage Tek

4c. Title: *Compilation Models for DSPS.* Speaker: Tom Conte, N.C. State University

4d. Title: *3rd Generation Cell Phone Base Station Beam Former Applications for BOPS & DSP.* Speaker: Dave Strube

Tuesday afternoon:

Free for individual interaction, recreation and planning.

8:00pm - 10:30pm

Session 5: Digital Information Appliances in Consumer Space

Session Chairs: John O'Donnell, Michinori Nishihara

5a. Title: *RF Technology for Consumer Space.* Speaker: Ray Barrett, Motorola

5b. Title: *TBD.* Speaker: Peter Dribble, Microware

5c. Title: *Information Appliances in Multimedia Networks, (90 minutes).* Speaker: Yuichiro Takagawa, NTT East

Title: IRDA-ISDN Pay Phone System

Short Talk 2: Ryuchi Saithoh, NTT

Wednesday, June 28

8:30am - 12:00 noon

Session 6: Multithreading & Microprocessor Arch. Innovations

Session Chairs: Allan Knies, Bob Montoye

6a. Title: *Transmeta Crusoe.* Speaker: Godfrey D'Souza, Transmeta

6b. Title: *AS/400 and RS/6000 System Architecture.* Speaker: Rick Eickemeyer, IBM

6c. Title: *Speculative Multi-threading in MAJC.* Speaker: Marc Tremblay, Sun

6d. Title: *SMT, SMP, and the Compaq 21464.* Speaker: Mathew Reilly

2000 IEEE Computer Elements Vail Workshop

June 25 -28, 2000

Invitation

The IEEE Technical Committee Elements invites you to participate in the 2000 Computer Elements Workshop to be held in Vail, Colorado from June 25 to June 28, 2000 at the Christiania Lodge on Hansen Ranch Road in Vail. An excellent program has been created by the program committee under the able leadership program chair Joel Boney.

The program starts at 5:00 p.m. on Sunday June 25. We hold the keynote address on Sunday evening, and have six sessions over the next three days. We encourage all attendees to contribute to the success of the workshop through their active participation. This could occur during discussion periods after the talks, at breaks, and at meals. This workshop has been structured to allow many opportunities for informal technical discussions. As in the past, we will continue to have an environment which allows an undocumented exchange of leading edge technical experiences from which al attendees can benefit. In accordance with IEEE workshop rules, no material will be published, nor will cameras or tape recorders be permitted. No proprietary information will be discussed, however, questions of technical nature may be discussed at length.

Attendance will be limited to ensure a workshop atmosphere, so please get your registration in early! The program for the workshop and registration information is on the following pages. The program is quite firm, although there may be some changes in content or order of presentation. Participants are encouraged to attend the entire workshop; no partial registration is offered. More details can be found at our web page located at www.computer.org/tab/tclist/tcce.htm then click on Computer Elements. The total fee of $635 ($585 for IEEE members) covers the IEEE workshop registration fee, lodging, and all meals from Sunday dinner through Wednesday. Registration is due by June 5, 2000. After this date rooms may not be available. Please feel free to contact the Registrar, John Polhemus (303-781-6190) for information or questions. I look forward to seeing you at the workshop for an interesting and fruitful exchange of ideas.

Van service from the Denver airport can be arranged by calling Colorado Mountain Express at 800-525-6363.

Please check the box to join the Computer Elements Technical committee. It costs nothing and demonstrates to the Computer Society that we are a technically interesting group to belong to.

Thank you,

Jerry Merckel
Chairman, IEEE Technical Committee on Computer Elements
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Contacts

Contacts for the 2000 Vail Computer Elements Workshop chairs are available on the Vail 2000 contacts page.

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Jerry Merckel, University of North Florida
Joel Boney, HP
Frank Mikalauskas, Compaq
John Polhemus, Consultant
Ron Bell, LSI Logic
Douglas Westcott, IBM
Michinori Nishihara,IBM

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If you have any comments or suggestions regarding the Computer Elements web page, please send an e-mail to:
gmerckel@unf.edu

Workshop

The 2001 Vail Computer Elements

Vail, Colorado

June 24-27, 2001

Sponsored by

IEEE Computer Society

The following is the outline of sessions for the Vail 2001 workshop as of March, 2001.

For further information please contact:
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Sunday Afternoon / Evening, June 24

4:00pm - 5:00pm - Technical Committee Meeting in Sarah's Lounge (all welcome)

5:00pm - Social Hour Followed by Dinner

8:00 pm - Evening Keynote Addressi given by:

Bob Guernsey, IBM & Allan Knies, Intel

- Three Perspectives on the technological future and how it will change our lives.
  Rich Gold, Xerox PARC
  William Pulleyblank, IBM
  Ted Selker, MIT Media Lab

Monday, June 25

8:15 am - 8:30 am - Announcements and Introductions

8:30 am - 12:00 noon

Session 1 - Communications

Ray Barrett, Consultant & David Baker, BOPS

- VOIP-Voice Over the Internet
  James A. Simak, ECI Telecom
- Communication Trends
  Ray Barrett, Consultant

- VOIP Real Time Frameworks
  Frank Barry, BOPS
- Orthogonal FDM for Wireless Networks
  Ali Sadri, BOPS

1:00 pm - 4:30 pm

Session 2: Servers

Linton Ward, IBM & Alan Charlesworth, Sun Microsystems

- Server Directions
  Alan Charlesworth, Sun Microsystems
- Modular Servers
  Dave Bottom, Intel
- Quantum Devices
  Rahim Khoie, University of North Florida
- Sun Fire Servers
  Alan Charlesworth, Sun Microsystems

8:00 pm - 10:00 pm

Session 3: Crypto

Jim Hughes, Storage Tek & Jack Bigham, General Dynamics Electronics Sys.

- Cryptography In Systems
  James P. Hughes, Storage Technology Corp.
- Factoring Large Numbers
  Paul C. Leyland, Microsoft Research Ltd.
- High Performance Computer Architecture
  Michael H. Merrill, National Security Agency
- Quantum Computing -Security of Public-Key Encryption Systems
  Tatsuaki Okamoto, NTT Labs

Tuesday, June 26

8:15 - 8:30 - Announcements

8:30 am - 12:00 noon

Session 4: Display Technology & Human Interface

Michinori Nishihara, IBM & Zenzo Tajima, Hitachi

- TFT Displays for PCs
  Zenzo Tajima, Hitachi
- TFT Displays for Industrial Applications

Shigehiko Satoh, NEC

- Organic Light Emitting Diodes
  David J. Williams, Eastman Kodak
- MicroDisplay Technology
  for Near-Eye Computer Applications
  Rajan Kapur, Zight

Tuesday afternoon:

Free for individual interaction, recreation and planning.

8:00pm - 10:30pm

Session 5: Radical New Storage

Robert Montoye, IBM & Renato Recio, IBM

- Extremely High Density Magnetic Recording
  Yoshimasa Miura, Fujitsu
- Limits of Magnetic Recording
  David Thompson, IBM
- Probe Storage
  Marty Frary, Storage Technologies
- Storage Technology Trends
  Rumi Zahir, Intel

Wednesday, June 27

8:30am - 12:00 noon

Session 6: Internet Appliances

John Sell, AMD & Dave Strube, BOPS

- PDA Video Processing
  Doina Petrescu, BOPS
- The Digital Home
  Don Gray, Microsoft
- Internet Appliance Applications
  John Alexander, University of North Florida
- Wireless Internet Requirements
  Dave Strube, BOPS

Contacts & Registration

Contacts for the 2001 Vail Computer Elements Workshop chairs are available on the Vail 2001 contacts page.

Steering Committee:
Jeff Yetter, Hewlett Packard
Jerry Merckel, University of North Florida
Joel Boney, HP
Frank Mikalauskas, Compaq
John Polhemus, Consultant
Ron Bell, MicroLinear
Douglas Westcott, IBM
Michinori Nishihara,IBM

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Last Updated: July, 2000
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This site designed and maintained by: katzfishy@aol.com

Workshop

The 2002 Vail Computer Elements

Vail, Colorado

June 23-26, 2002

Sponsored by

IEEE Computer Society

The following is the outline of sessions for the Vail 2002 workshop.

For further information please contact:
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Fax: (763) 424-1776
Email: jim@network.com

Invitation & Registration

Design Challenges

Program Chair: R. Brad Older, Intel
Program Co-Chair: James Hughes, Storage Tek

Sunday, June 23

5:00pm - Social Hour followed by dinner & Keynote Presentation.

"The Road to 64 Bits: Intel/HP vs AMD"
Bill Worley, HP & Allan Knies, Intel - Fred Weber, AMD & Wayne Meretsky, AMD.
Moderator Jim Slager, JAZiO

Monday, June 24

Session 1	New Microprocessors	Chairs Jim Slager & Chris Malachowsky
1.1	Intel/HP McKinley	Terry Lyon, HP
1.2	AMD Sledge Hammer	Fred Weber,AMD
1.3	NVIDIA GeForce 4	John Montrym, NVIDIA
1.4	Complexity vs Power vs Performance	Carl Anderson, IBM
Session 2	SOC & SOI	Chairs David Baker & Robert Montoye
2.1	Vertical ICs via Through Silicon	Pat Halahan, Tru-Si
2.2	Advances in SOI	Rahim Khoie, UNF
2.3	SOC Development Methodologies	Oscar Mitchell, LayerN
2.4	SOC Development for AU1500	Rich Witek, Alchemy
Session 3	Internet & Wireless	Chairs James Simak & Ray Barrett
3.1	Lower Power Spread Spectrum	Ron Bell, Micro Linear

3.2	Ad Hoc Networks	Ed Callaway, Motorola
3.3	Internet Road Weather System	David Lambert, UNF
3.4	Multimedia on the Internet	Horst Clausen, Univ. of Salzburg

Tuesday, June 25

Session 4	Consumer Electronics	Chairs Michinori Nishihara & Yokshiiaki Hagiwara
4.1	Palm Directions	Bill Stanely, Palm
4.2	Software System on a Chip	Dave Fotland, Ubicom
4.3	Consumer Electronics Trends	Yoshiiaki Hagiwara, Sony
4.4	Digital Video Trends	George Cooper, Adtec
Session 5	Embedded & Mixed Signal Systems	Chairs Allan Knies & John Alexander
5.1	RF Circuits in a CMOS Design	Stephen Pawlowski, Intel
5.2	MAP BSP-15	Chris Basoglu, Equator
5.3	Embedded Intelligent Sensors	John Alexander, UNF

Wednesday, June 26

Session 6	Systems Interconnect & Packaging	Chair Alan Charlesworth
6.1	Server Revenue Trends	Alan Charlesworth, Sun
6.2	SMP Technology	Alan Charlesworth, Sun
6.3	I/O Wars: 3GIO/Infiniband/IP Off-load	Greg Pfister, IBM
6.4	Gigabit Ethernet Mesh	Ravi Kavuri, StorageTek

Contacts

Contacts for the 2002 Vail Computer Elements Workshop chairs are available on the Vail 2002 contacts page.

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Frank Mikalauskas, Compaq
John Polhemus, Consultant
Ron Bell, MicroLinear
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Last Updated: 03 May 2002

Workshop
The 2003 Vail Computer Elements

Vail, Colorado
June 22-25, 2003

Sponsored by
IEEE Computer Society

The following is the outline of sessions for the Vail 2003 workshop.
If you are interested in making a presentation, please contact the session chair.

For further information please contact:

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Phone: (763) 424-1676
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Email: james_hughes@storagetek.com

Expanding Horizons

Program Chair: James Hughes, Storage Tek, james_hughes@storagetek.com
Program Co-Chair: R. Brad Older, Intel, brad.older@intel.com

Sunday, June 22 - Social hour followed by dinner & Keynote Presentation.

"Privacy & Security," Valerie McNevim, State of Colorado
Keynote Chair: Ron Bell, Micro Linear, bell.ron@microlinear.com

Monday, June 23

Session 1 — PROCESSORS
Chair: Jim Slager, Jazio, jslager@jazio.com
Chair: Carl Anderson, IBM, cja@us.ibm.com

1.1 Tera-op Adaptive Processing, Chuck Moore, U. of Texas
1.2 Future Server Processors, Brad McCredie, IBM
1.3 Dual Core Itanium Power Management, Sam Naffziger, HP
1.4 Future Microprocessors, Jim Kahle, IBM

Session 2 — SECURITY
Chair: Bill Worley, NextGenInet, worley@nextgeninet.com
Chair: Jim Hughes, Storage Tek, james_hughes@storagetek.com

2.1 OS Security, Brian LaMacchia, Microsoft
2.2 Cybercrime, Dave Mahon, FBI

2.3 Storage Encryption, Jim Hughes, Storage Tek
2.4 Signature Only Smart Cart, Lynn Wheeler, FirstData

Session 3 SYSTEM POWER ISSUES
Chair: Ray Barrett, Maxim, rlb@design.mxim.com
Chair: Bob Montoye, IBM, montoye@us.ibm.com
3.1 CPU Power Design, Ray Barrett, Maxim
3.2 Powering Handheld Displays, Alex Gusinov, Sipex
3.3 System On Chip, Subramanian Iyer, IBM
3.4 Portable Systems, Bob Montoye, IBM

Tuesday, June 24

Session 4 CONSUMER ELECTRONICS
Chair: Michinori Nishihara, IBM, michi@jp.ibm.com
Chair: Yoshiaki Hagiwara, Sony, yoshiaki.hagiwara@jp.sony.com
4.1 AI in Strategy Games, David Fotland, Smart Games
4.2 Portable Phone Directions, Makoto Miyake, Mitsubishi
4.3 Networked Entertainment, Naohisa Ohta, Sony
4.4 Low Power Electronics, Rahim Khoie, U. of the Pacific

Session 5 COMMUNICATIONS
Chair: Ed Callaway, Motorola, Ed.callaway@motorola.com
Chair: Ravi Kavuri, StorageTek, Ravi_kavuri@storagetek.com
5.1 IEEE 802.15.4 RF Transceiver, Fred Martin, Motorola
5.2 MASI Comm Processor, David Fotland, Ubicom
5.3 Ultra-Wideband Comm Systems, Roberto Aiello, Discrete Time
5.4 Gb Ethernet, Atiq Ahamad, StorageTek

Wednesday, June 25

Session 6 SYSTEMS
Chair: Alan Charlesworth, Sun, Alan.charlesworth@sun.com
Chair: Dave Baker, A6Labs, Db@a6labs.com
6.1 Large Server Trends, Alan Charlesworth, Sun
6.2 Embedded Systems, Tom Conte, NC State Univ.
6.3 SOC IP SAN, Gary McMillian, aRTiCA Semiconductor
6.4 Tera-Tory Processor, David Baker, A6Labs

Contacts

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Jerry Merckel, University of North Florida

Jim Hughes, StorageTek
Frank Mikalauskas, Hewlett-Packard
John Polhemus, Consultant
Ron Bell, Micro Linear
Michinori Nishihara, IBM

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Updated: 01-May-2003

If you have any comments or suggestions regarding the Computer Elements web page, please send an e-mail to gmerckel@unf.edu.

Workshop
IEEE 2004 Vail Computer Elements

Vail, Colorado
June 27-30, 2004

Sponsored by
IEEE Computer Society

The following is the outline of sessions for the Vail 2004 workshop.
If you are interested in making a presentation, please contact the session chair.

For further information please contact:

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Future Visions

Program Chair: Tom Conte, NC State University, conte@ncsu.edu
Program Co-Chair: James Hughes, Storage Tek, james_hughes@storagetek.com

Sunday, June 27 - Social hour followed by dinner & Keynote Presentation.

Visual Perception and Reality

Speaker: Dr. William Glenn, Florida Atlantic University, glenn@fau.edu
Keynote Chair: Ron Bell, Math Star, ron.bell@mathstar.com

Monday, June 28

Session 1 — PROCESSORS
Chair: Jim Slager, SuperH, jslager@iname.com
Chair: Carl Anderson, IBM, cja@us.ibm.com

1.1 Power 5
Mark Sweet, IBM

1.2 UltraSparc IV
Quinn Jacobson, Sun Microsystems

1.3 Fast14 Technology
Mike Becker, Intrinsity

1.4 Pentium 4 Prescott
Ronak Singhal, Intel

Session 2 — Panel: FPGAs vs. ASICS Panel

Chair: Ron Bell, MathStar, ron.bell@mathstar.com
Chair: Bill Mangione-Smith, UCLA, billms@ee.ucla.edu

2.1 Re-configurable Directions
Cary Snyder, SemiView

2.2 Embedded FPGA Apps
Parimal Patel, Xilinx

2.3 FPGA/ASIC Design Flow
David Taubenheim, Motorola

2.4 Adaptive Computing Processor
Paul Master, QuickSilver

2.5 Re-configurable Design
Ron Bell, MathStar

Session 3

ADV. SEMICONDUCTOR TOOLS
Chair: Robert Guernsey, IBM, guernsey@us.ibm.com
Chair: Subramanian Iyer, IBM, ssiyer@us.ibm.com

3.1 EDA Challenges
Ted Vucurevich, Cadence

3.2 Analysis & Process Variability
Leon Stok, IBM

3.3 Design for Yield Management
Andrzej Strojwas

Tuesday, June 29

Session 4

CONSUMER ELECTRONICS
Chair: Michinori Nishihara, IBM, michi@jp.ibm.com
Chair: Yoshiaki Hagiwara, Sony, yoshiaki.hagiwara@jp.sony.com

4.1 DVD Player Technology
Hiroki Mouri, Panasonic

4.2 Mobile Multimedia Processor
Kunio Uchiyama, Hitachi

4.3 MPU for Consumer Apps
Naoki Mitsuishi, Renesas

4.4 Processor Design Trade-offs
Peter Hofstee, IBM

Session 5

Panel: BLADES vs. SMP Panel
Chair: Alan Charlesworth, Sun, alan.charlesworth@sun.com
Chair: Richard Oehler, NEWISYS, rich.oehler@newisys.com

5.1 Alan Charlesworth, Sun Microsystems

5.2 Linton Ward, IBM

5.3 Tom Barclay, Microsoft

5.4 Bruce Lindsay, IBM

5.5 Rich Adkisson, HP

Wednesday, June 30

Session 6 — WIRELESS

Chair: Ed Callaway, Motorola, ed.callaway@motorola.com
Chair: Kevin Doren, kevin@doren.org

6.1 Software Defined Radio
John Grosspietsch, Motorola

6.2 UWB Communications
Robert Aiello, Staccato Communications

6.3 UWB Propagation
Kai Siwiak, Time Derivative

6.4 The ZigBee Spec
Robert Heile, The ZigBee Alliance

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Frank Mikalauskas, Hewlett-Packard
John Polhemus, Consultant
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Updated: 16-Jul-2003

If you have any comments or suggestions regarding the Computer Elements web page, please send an e-mail to gmerckel@unf.edu.

Workshop

IEEE 2005 Vail Computer Elements

Vail, Colorado
June 26-29, 2005

Sponsored by

IEEE Computer Society

The following is the outline of sessions for the Vail 2005 workshop.

If you are interested in making a presentation, please contact the session chair.

For further information please contact:

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Future Visions

Program Chair: Allan Knies, Intel, allan.knies@intel.com
Program Co-Chair: Tom Conte, NC State University, conte@ncsu.edu

Sunday, June 26 - Social hour followed by dinner & Keynote Presentation.

Intelligent DRAM - Challenges & Opportunities

Speaker: Peter Hsu, Consultant, peterhsu@cs.wisc.edu
Keynote Chair: Bill Mangione-Smith, UCLA, billms@ucla.edu

Monday, June 27

Session 1 — POWER & PACKAGING
Chair: Ray Barrett, Maxim, rlb@design.mxim.com
Chair: Bradley McCredie, IBM, mccredie@us.ibm.com

1.1 Thermal Design: Workstations & Servers, Andy Delano, HP

1.2 3D Packaging Trends, Bob Patti, Tezzaron

1.3 Military & Space Power, Jack McGirr , AKE

1.4 System Power & Cooling, Mike Nealon, IBM

Session 2 — Panel: BEYOND MOORE'S LAW
Chair: Carl Anderson, IBM, cja@us.ibm.com

Chair: James Hughes, StorageTek, James_Hughes@storagetek.com

2.1 CMOS Technology Perspective, Emmanuel Crabbe, IBM

2.2 Design Perspectives, Stefan Rusu, Intel
2.3 Future Systems Perspective, Rich Oehler, AMD

2.4 LP CMOS via Probabilistic Computing, Krishna Palem, GA Inst. of Tech

Session 3 EMBEDDED PROCESSORS
Chair: Jim Slager, SuperH, jslager@iname.com
Chair: Tom Conte, NC State University, conte@ncsu.edu
3.1 New NAND Gate: Xtensa Processor, Bill Huffman,, Tensilica
3.2 PowerPC Architectural Advancements, Pete Wilson, Freescale
3.3 3D Media Processor, Gerrit Slavenburg, NVIDIA

Tuesday, June 28

Session 4 CONSUMER ELECTRONICS
Chair: Michinori Nishihara, IBM, michi@jp.ibm.com
Chair: Yoshiaki Hagiwara, Sony, yoshiaki.hagiwara@jp.sony.com
4.1 10 Gbps Wireless Millimiter Waves, Takao Nagatsuma, NTT
4.2 Imager Sensor Technology, Hirofumi Sumi, Sony
4.3 Next Generation DVD Codec, Tetsuya Hara, Renesas Technology
4.4 Cell Processor Programming Features, Barry Minor, IBM

Session 5 PETAFLOPS SYSTEM TRADEOFFS PANEL
High Productivity Computing Systems
Chair: Alan Charlesworth, Sun, alan.charlesworth@sun.com
Chair: Robert Guernsey, IBM, guernsey@us.ibm.com

5.1 IBM HPCS Panelist, Balaram Sinharoy

5.2 Cray HPCS Panelist, Mike Parker
5.3 Sun HPCS Panelist, Brian O'Krafka
5.4 SGI HPCS Panelist, Steve Miller, SGI
5.5 IBM HPCS Panelist, Jeff Burns, IBM

Wednesday, June 29

Session 6 LOW POWER WIRELESS COMMUNICATIONS
Chair: Ed Callaway, Motorola, ed.callaway@motorola.com
Chair: Bob Montoye, IBM, montoye@us.ibm.com
6.1 LP Rad Tolerant CPU, Jody Gambles, U. of Idaho

6.2 LP via Scaling, Leland Chang, IBM

6.3 Energy Scavenging Technologies, Rajeevan Amirtharajah, UC Davis

6.4 Space Flight Telecommunications
Chris Haskins & Wes Millard , Johns Hopkins Univ.

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Updated: 31-Mar-2005

If you have any comments or suggestions regarding the Computer Elements web page, please send an e-mail to gmerckel@unf.edu.

IEEE Computer Society

2006 VAIL Computer Elements Workshop

June 25-28, 2006

New Horizons

Program Chair Dale Morris, HP
Dale.morris@hp.com
Program Co-Chair Allan Knies, Intel
Allan.knies@intel.com

Sunday June 25 5 PM Registration followed by Dinner and Keynote Presentation

8:00 PM – 9:15 PM

"Intellectual Property" , TBD Speaker

Keynote Chair Tom Conte, NC State University
conte@ncsu.edu

Monday June 26

8:30 AM – 12:00 noon

Session 1: High Perf. Clusters — Chairs Carl Anderson, IBM & Rich Oehler, AMD
cja@us.ibm.com rich.oehler@amd.com

1:00 PM – 4:30 PM

Session 2: Parallelizing Applications — Chairs Bill Huffman, Tensilica & Jeff Burns, IBM
Huffman@tensilica.com jlburns@us.ibm.com

8:00 PM – 10:15 PM

Session 3: Code Gen & Design Auto — Chairs Tom Conte, NC St Univ & Damir Jamsek, IBM
conte@ncsu.edu jamsek@us.ibm.com

Tuesday June 27

8:30 AM – 12:00 noon

Session 4: Consumer Electronics — Chairs Atsushi Hasegawa, Renesas & Hirofumi Sumi, Sony
Hasegawa.atsushi@renesas.com Hirofumi.Sumi@jp.sony.com

8:00 PM – 10:15 PM

Session 5: Security & Authentication — Chairs Jim Hughes, StorageTek & Lynn Wheeler, First Data
James_Hughes@storagetek.com lynn@garlic.com

Wednesday June 28

8:30 AM – 12:00 noon

Session 6: Gaming — Chairs Robert Montoye, IBM & Peter Hsu, Consultant
montoye@us.ibm.com peterhsu@cs.wisc.edu

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Vice Chair **Jerry Merckel** gmerckel@unf.edu

Registration Chair **Ron Bell**; Ron.bell@mathstar.com
Asia Pacific Chair Michi Nishihara michi@jp.ibm.com

Finance Chair **John T. Polhemus** jtpolhemus@msn.com
Database Jerry Dixon jerrydixon@cfl.rr.com

IEEE Computer Society
2007 VAIL Computer Elements Workshop
June 24-27, 2007

2010 & Beyond

Program Chair: Jay Fleischman, AMD **jay.fleischman@amd.com**
Program Co-Chair: Dale Morris, HP **Dale.morris@hp.com**

Sunday June 24 5 PM Registration, Dinner and Keynote Presentation, **8:00 PM – 9:15 PM**

RAMP: Research Accelerator for Multiple Processors
Community Vision for a Shared Experimental Parallel HW/SW Platform
John Wawrzynek [johnw@eecs.berkeley.edu]

Keynote Chair Allan Knies, Intel **Allan.knies@intel.com**

Monday June 25

Session 1: CPUs Chairs Steve Miller, NetApp & Bill Huffman, Tensilica
8:30 AM – 12:00 noon **scm@netapp.com** **Huffman@tensilica.com**
1.1 Computer Processing – Next Step Bill Harrod, DARPA, william.harrod@darpa.mil
1.2 Architecture: SW Transactional Memory Ali-Reza Adl-Tabatabai Intel, ali-reza.adl-tabatabai@intel.com
1.3 CPU ROCK Marc Tremblay, Sun, marc.tremblay@sun.com
1.4 Power 6 Bill Huott, IBM, huott@us.ibm.com

Session 2: Memory Chairs Bob Patti, Tezzaron & Jeff Burns, IBM
1:00 PM – 4:30 PM **rpatti@tezzaron.com** **jlburns@us.ibm.com**
2.1 High Performance SOI eDRAM John Barth, IBM , jbarth@us.ibm.com
2.2 DRAM – Past, Present & Future Fred Jones, United Memory, fred@unimem.com
2.3 Emerging Non-Volatile Memories Bill Gallagher, IBM, glgr@us.ibm.com
2.4 3D – IC Memory Bob Patti, Tezzaron, rpatti@tezzaron.com

Session 3: Enterprise System Trends Chairs Lynn Wheeler, Wheeler & Wheeler & Robert Guernsey, IBM
8:00 PM – 10:15 PM **lynn@garlic.com** **Guernsey@us.ibm.com**
3.1 3D Internet – Enterprise Enterverse Jon Watte, Forterra Systems, jwatte@forterrainc.com
3.2 Blades: Edge to Enterprise Migration Kirk Bresniker, HP, kirk.bresniker@hp.com
3.3 Next Generation Computing Systems David LaPotin, IBM, dpl@us.ibm.com

Tuesday June 26

Session 4: Consumer Electronics & Robots Chairs Atsushi Hasegawa, Renesas & Hirofumi Sumi, Sony
8:30 AM – 12:00 noon **Hasegawa.atsushi@renesas.com** **Hirofumi.Sumi@jp.sony.com**
4.1 Wireless 10Gbs – Uncompressed HDTV Yoichi Kado, NTT, kado@aecl.ntt.co.jp
4.2 Robot Electronics & Info Processing Toshihiro Matsui, AIST Dig. Human Research Ctr., t.matsui@aist.go.jp
4.3 Pwr Control for Self-Synchronous System Makoto Ikeda, U of Tokyo, ikeda@silicon.t.u-tokyo.ac.jp
4.2 DSC Industry Evolution Yaichi Aoshima, Hitotsubashi Univ., aoshima@iir.hit-u.ac.jp

Session 5: Highly Threaded OS/HyperVis. Chairs Jim Hughes, Sun & Ron Perez, IBM
8:00 PM – 10:15 PM **james.hughes@sun.com** **ronpz@us.ibm.com**
5.1 Support for High Thread Counts in Solaris Bart Smaalders, Sun, bart.smaalders@sun.com
5.2 Hardware Virtualization Trends Leendert van Doorn AMD, leendert.vandoorn@amd.com
5.3 Scalability in System Software Dilma Da Silva, IBM, dilmasilva@us.ibm.com

Wednesday June 27

Session 6: Wireless & Ad Hoc Networks Chairs Ed Callaway, Motorola & Tom Conte, NC State Univ.
8:30 AM – 12:00 noon **ed.callaway@motorola.com** **conte@ncsu.edu**
6.1 Cognitive Radio Trends Ed Callaway, Motorola, ed.callaway@motorola.com
6.1 Policy-based Radios Preston Marshall, DARPA ATO, preston.marshall@darpa.mil
6.2 Cellular Ad hoc Networks Michael Johnson, Motorola, mike.johnson@motorola.com
6.3 Multi-Standard Radio: Are We There Yet? Jim Lansford, Alereon, jim.lansford@alereon.com

Arrangements Chair **John M. Polhemus** **John.m.polhemus@lmco.com**
Registration Chair **Ron Bell** **Ron.bell@mathstar.com**
Finance Chair **John T. Polhemus** **jtpolhemus@msn.com**

The 3D Internet: An Enterverse For The Enterprise"

IEEE Computer Society
2008 VAIL Computer Elements Workshop
June 22-25, 2008

What's New?

Program Chair: Steve Miller, NetApp, **scm@netapp.com**
Program Co-Chair: Jay Fleischman, AMD, **jay.fleischman@amd.com**

Sunday June 22 5 PM Registration, Dinner and Keynote Presentation, **8:00 PM – 9:15 PM**

"The Future is Parallel: What's a programmer to do?"
Guy Steele, Sun Microsystems, **guy.steele@sun.com**

Keynote Chair Jim Hughes, Sun, **james.hughes@sun.com**

Monday June 23

Session 1: Intelligent Networks — Chairs David LaPotin, IBM & Rick McGeer, HP Labs
8:30 AM – 12:00 noon — dpl@us.ibm.com, rick.mcgeer@hp.com

1.1 OptiPlanet–Global Computing Via Light Paths	Jason Leigh **,** Univ of Illinois, spiff@uic.edu
1.2 Global Envir for Network Investigations	Chip Elliott, BBN Technologies, celliott@bbn.com
1.3 Network Evolution: Tech & Applications	Charles Kalmanek, AT&T Labs, **crk@research.att.com**
1.4 Military Communications & Networking	Kenneth Young, Telcordia, kcy@research.telcordia.com

Session 2: Next Gen Database Systems — Chairs Damir Jamsek, IBM & Bob Lucas, USC
1:00 PM – 4:30 PM — jamsek@us.ibm.com, rflucas@isi.edu

2.1 Blue Gene	Todd Takken, IBM, takken@us.ibm.com
2.2 Super Computing & Mainstream Components	Richard Kaufmann, HP, Richard.kaufmann@hp.com
2.3 Roadrunner-Heterogeneous Supercomputing	John Morrison, Los Alamos National Laboratory, jfm@lanl.gov
2.4 Programming for Super Parallel Computing	Koh Hotta, Fujitsu, hotta@jp.fujitsu.com

Session 3: Cognitive Computing & User I/Fs — Chairs Dale Morris, HP & Niraj Srivastava, HP
8:00 PM – 10:15 PM — dale.morris@hp.com, niraj.srivastava@hp.com

3.1 Data Center Management User Interface	Kostadis Roussos, NetApp, kostadis.roussos@netapp.com
3.2 Computers for Cognition	Richard Lethin, Reservoir Labs, lethin@reservoir.com
3.3 I/F Design – The Good, Bad & Ugly	Mark Anspach, HP, mark.anspach@hp.com

Tuesday June 24

Session 4: Displays & Packaging — Chairs Atsushi Hasegawa, Renesas & Hirofumi Sumi, Sony
8:30 AM – 12:00 noon — Hasegawa.atsushi@renesas.com, Hirofumi.Sumi@jp.sony.com

4.1 System LSI for Digital Broadcasting Apps	Jiro Naganuma, NTT Cyber Space Lab, naganuma.jiro@lab.ntt.co.jp
4.2 Electronic Paper Network System	Reiji Hattori, Kyushu University, hattori@ed.kyushu-u.ac.jp
4.3 Organic Electronics on Plastic Films	Jiro Kasahara, Sony, jiro.kasahara@jp.sony.com
4.4 Multi-layer Stacked Devices Fabrication	Nobuaki Miyakawa, Honda Research Inst., miyakawa@jp.honda-ri.com

Session 5: Embedded Systems & Apps — Chairs Mario Vinsani, ERIX & Craig Shinners, MIPS
8:00 PM – 10:15 PM — Mario.vinsani@tiscalinet.it, craig@mips.com

5.1 Multi-threaded Multi-core Embedded Systems	Kevin D. Kissell, Paralogos S.A.R.L, kevink@paralogos.com
5.2 MIPS 74K 1GHz+	Jack Brown, MIPS, jackb@mips.com
5.3 Skyplex Satellite Terminal Design	Peter Maurutschek, Global Comm. & Service, pmm@cosy.sbg.ac.at
5.4 European Research-Embedded Systems	Mario Vinsani, ERIX, Mario.vinsani@tiscali.it

Wednesday June 25

Session 6: Future Technologies — Chairs Ray Barrett, Allegro & Bill Gallagher, IBM
8:30 AM – 12:00 noon — rbarrett@allegromicro.com, glgr@us.ibm.com

6.1 Nanoelectronics Research Challenges	Jeff Welser, Nanoelectronics Research Inst., jeff.welser@src.org
6.2 Carbon-based Electronics	Shalom Wind, Columbia University, sw2128@columbia.edu
6.3 Quantum Computing	Matthias Steffen, IBM, msteffe@us.ibm.com
6.4 Spintronics	Russell Cowburn, Imperial College London, r.cowburn@imperial.ac.uk

Arrangements Chair **John M. Polhemus**
John.m.polhemus@lmco.com

Registration Chair **Ron Bell**
ron.bell@brin.com

Finance Chair **John T. Polhemus**
jtpolhemus@msn.com

IEEE Computer Society
2009 VAIL Computer Elements Workshop
June 21-24, 2009

The Next 40 Years

Program Chair: Bill Huffman, Tensilica, huffman@tensilica.com
Program Co-Chair: Steve Miller, NetApp, scm@netapp.com

Sunday June 21 5 PM Registration, Dinner and Keynote Presentation, **8:00 PM – 9:15 PM**

"IEEE Vail – The Last 40 Years"

John Polhemus, jtpolhemus@msn.com , & Ron Bell, ron.bell@brin.com

Monday June 22

Session 1: Processors — **Chairs Yahya Sotoudeh, Intel, & Allan Knies, Intel**
8:30 AM – 12:00 noon — yahya.sotoudeh@intel.com allan.knies@intel.com
1.1 Godson 3 — Weiwu Hu, ICT, hww@ict.ac.cn
1.2 Nhm-EX — Jeff Baxter, Intel, jeff.baxter@intel.com
1.3 Fusion Processor Challenges — Sebastien Nussbaum, AMD, sebastien.nussbaum@amd.com
1.4 Rainbow Falls — **Ricky Hetherington, Sun, ricky.hetherington@sun.com**

Session 2: Heterogeneous Multi-core & Graphics **Chairs Damir Jamsek, IBM, & Jay Fleischman, AMD**
1:00 PM – 4:30 PM — jamsek@us.ibm.com jay.fleischman@amd.com
2.1 Anton Machine — Marty Deneroff, Deshaw Research, Marty.Deneroff@DEShawResearch.com
2.2 Accelerated Computing — Chuck Moore, AMD, chuck.moore@amd.com
2.3 AMD StreamTM – Parallel Computing — Michael Mantor, AMD, Michael.mantor@amd.com
2.4 Video/Graphics Computing — Steve Parker, Nvidia, sparker@nvidia.com

Session 3: Disruptive Technology — **Chairs Kevin Kissell, Paralogos SARL & Jim Mitchell, Sun**
8:00 PM – 10:15 PM — **kevink@paralogos.com** **jim.mitchell@sun.com**
3.1 Silicon Photonics Interconnects — Ashok Krishnamoorthy, Sun, ashok.krishnamoorthy@sun.com
3.2 Moore's Law Means Multi-core — Niraj Srivastava, Interactive Supercomputing
-------- — nsrivastava@interactivesupercomputing.com
3.3 Multi-core API & Compiler Technology — Hironori Kasahara, Waseda Univ, kasahara@waseda.jp

Tuesday June 23

Session 4: Consumer Electronics — **Chairs Fumio Arakawa, Renesas & Hirofumi Sumi, Sony**
8:30 AM – 12:00 noon — arakawa.fumio@renesas.com Hirofumi.Sumi@jp.sony.com
4.1 NHK Super Camera Technology — Hiroshi Shimamoto, NHK Eng., shimamoto@nes.or.jp
4.2 TOMBO x, y, z, t, λ Resolution — Keiichiro Kagawa, Osaka Univ, kagawa@ist.osaka-u.ac.jp
4.3 Low Power Mobile Multi-core — Fumio Arakawa, Renesas Technology, arakawa.fumio@renesas.com
4.4 Real-world Robot Audition — Kazuhiro Nakadai, Honda Research, nakadai@jp.honda-ri.com

Planning Session: IEEE Vail 2010, 4PM – 5:30 PM **All invited to participate.**

Session 5: Green Systems & Power — **Chairs Ray Barrett, Allegro Micro, & Jesse Edwards, Global Cooling**
8:00 PM – 10:15 PM — **raybarrett@comcast.net** **jedwards@globalcooling.com**
5.1 Open Source IP - Disruptive Innovation — Steve Wald, Acuitus, steve@acuitusengineering.co
5.2 Power Management for Green Computing — Ray Barrett, VLSI Consultant, raybarrett@comcast.net
5.3 "Green" Computing — Frank Drews, Ohio State Univ., drews@ohio.edu

Wednesday June 24

Session 6: Multi-core, Safety & Security SW — **Chairs Jim Hughes, Huawei N. America, & Yoshiiaki Hagihara, AIP Labs**
8:00 AM – 12:00 noon — **jhughes@huawei.com** **hagihara-yoshiaki@aiplab.com**
6.1 Itanium RAS Via Lockstep — Cameron McNairy, Intel, Cameron.mcnairy@intel.com
6.2 Transparent Multi-Core Crypto — **Christoph Schuba, Sun, christoph.schube@sun.com**
6.3 FireFly – New RISC ISA — Dave Baker, dbaker@alumni.utexas.net
6.4 Fujitsu SPARC64 VII RAS — Tsuyoshi Motokurumada, Fujitsu, motokurumada@jp.fujitsu.com

Arrangements Chair **John M. Polhemus** John.m.polhemus@lmco.com
Registration Chair **Ron Bell** ron.bell@brin.com
Finance Chair **John T. Polhemus** jtpolhemus@msn.com

IEEE Computer Society
2010 VAIL Computer Elements Workshop
June 27-30, 2010

New Horizons

Program Chair: Sam Naffziger, AMD, Samuel.naffziger@amd.com
Program Co-Chair: Bill Huffman, Tensilica, huffman@tensilica.com

Sunday June 27 5 PM Registration, Dinner and Keynote Presentation (**8:00 PM – 9:15 PM)**

"Intersection of Culture & Technology – Starting a High Tech Company"

Chair: Steve Miller, NetApp, scm@netapp.com Speaker: **Dave Hitz**, NetApp, dave.hitz@netapp.com

Monday June 28

Session 1: Software	Chairs Rich Lethin, Reservoir, & David Baker, Green Hills Software
8:30 AM – 12:00 noon	lethin@reservoir.com dbaker@ghs.com
1.1 Certified Software	Zhong Shao, Yale University, shao-zhong@cs.yale.edu
1.2 High Performance Secure Virtualization	Dan Hettena, GHS, danh@ghs.com
1.3 Multi-core Code Parallelization	Faraydon Karim, No Boundary Comp, faraydon.karim@noboundarycomputing.com
1.4 Compiler Mapping to Multi-GPUs	Nicolas Vasilache, Reservoir, vasilache@reservoir.com
1.5 Alias: Many-Core Fabric- CE & Embedded	Ben Cutler, Microsoft , ben@aliasdsp.com
Session 2: Semiconductor Trends	Chairs Yahya Sotoudeh, Intel, & Carl Anderson, IBM
1:00 PM – 4:30 PM	yahya.sotoudeh@intel.com cja@us.ibm.com
2.1 Foundry Trends	Andy Wei, Global Foundries, andy.wei@globalfoundries.com
2.2 Superconducting Computing Electronics	Robert Wisnieff, IBM, wisnieff@us.ibm.com
2.3 Phase Change Memory Overview	Roger Cheek, IBM, cheekrw@us.ibm.com
2.4 Ultra Low Power Processing Options	George Bourianoff, Intel, geroge.i.bourianoff@intel.com
Session 3: Memory & Storage	Chairs Jay Fleischman, AMD, & Jim Hughes, Huawei
8:00 PM – 10:15 PM	jay.fleischman@amd.com jhughes@huawei.com
3.1 Storage Class MEM-Tech & Sys Overview	Winfried Wilcke, IBM, winfriedwilcke@us.ibm.com
3.2 New MEM Storage Architectural Directions	Raju Bopardikar, HP, raju.c.bopardikar@hp.com
3.3 DRAM/Flash MEM Limits – 5 Year Outlook	Gary Bronner, Rambus, gbronner@rambus.com

Tuesday June 29

Session 4: Consumer Electronics	Chairs Atsushi Hasegawa, Renesas & Hirofumi Sumi, Sony
8:30 AM – 12:00 noon	hasegawa.atsushi@renesas.com Hirofumi.Sumi@jp.sony.com
4.1 Context-Aware Improved User Experience	Masato Edahiro, NEC, eda@bp.jp.nec.com
4.2 Dust-Size Batteryless Sensor Node	Mitsuru Harada, NTT, haradam@aeci.ntt.co.jp
4.3 Spin-RAM Development	TBD, AIST, TBD
4.4 Image Recognition Driver Assistance	TBD, Renesas, TBD

Planning Session: IEEE Vail 2011, 4PM – 5:30 PM All invited to participate.

Session 5: Data Centers	Chairs Sebastien Nussbaum, AMD & Herb Schorr, Univ. S. CA
8:00 PM – 10:15 PM	sebastien.nussbaum@amd.com schorr@isi.edu
5.1 Network Oriented Services	Steve Hunter, IBM, hunters@us.ibm.com
5.2 Cloud Computing	Stan Freck, stan.freck@microsoft.com;Hasan Alkhatib, hasanal@microsoft.com
5.3 Large Data Center Thermal/Electrical	Amir Michael, Facebook, amir@facebook.com

Wednesday June 30

Session 6: Biomedical & Human Interfaces	Chairs Ray Barrett, American R & D, & Steve Wald, Acuitus Tech,
8:00 AM – 12:00 noon	raybarrett@comcast.net swald@ieee.org
6.1 Bio-Medical Product Development	Ray Barrett, American R&D, raybarrett@comcast.net
6.2 Healthy/Unhealthy Biological Systems	Boris Golosarsky, MD/PhD, bgolor@gmail.com
6.3 3D Displays	Miller Schuck, RealD, mschuck@reald.com
6.4 Medical/Business Issues	Neil Bartlett, Signostics Medical, nbartlett@signosticsmedical.com

Arrangements Chair John M. Polhemus
John.m.polhemus@lmco.com

Registration Chair Ron Bell
ron.bell@brin.com

Finance Chair John T. Polhemus
jtpolhemus@msn.com

Committee Chair Jim Hughes
jhughes@huawei.com

Comm. Vice Chair Ray Barrett
raybarrett@comcast.net

Asia Pacific Chair Atsushi Hasegawa
hasegawa.atsushi@renesas.com

IEEE Computer Society
2011 VAIL Computer Elements Workshop
June 26-29, 2011

Expanding Frontiers

Program Chair: Yahya Sotoudeh, Intel, yahya.sotoudeh@intel.com
Program Co-Chair: Sam Naffziger, AMD, Samuel.naffziger@amd.com

Sunday June 26 5 PM Registration, Dinner and Keynote Presentation (**8:00 PM – 9:15 PM)**

Throughways, By-ways and Cul-de-sacs

Key Note Chair: Jim Hughes, jhughes@huawei.com Key Note Speaker: Dr. Anita Jones, jones@cs.virginia.edu

Monday June 27

Session 1: Processors	Chairs Sam Naffziger, AMD, & Steve Miller, NetApp
8:30 AM – 12:00 noon	Samuel.naffziger@amd.com scm@netapp.com
1.1 Bobcat – Low Power Processor	Brad Burgess, AMD, brad.burgess@amd.com
1.2 Server Storage Convergence	Mike McGrath, Intel, Michael.mcgrath@intel.com
1.3 Low Power TI MSP 430 with FRAM	Christy She, TI, c-she@TI.com
1.4 IBM z196 Microarchitecture	Eric Schwarz, IBM, eschwarz@us.ibm.com
Session 2: **High Performance Wireless**	Chairs Bill Huffman, Tensilica, & Ray Barrett, American R & D
1:00 PM – 4:30 PM	huffman@tensilica.com raybarrett@comcast.net
2.1 Multi-Protocol SW Radio	Andrzej Rucinski, Univ. New Hampshire, andrzej.rucinski@unh.edu
2.2 MIMO for Reliable Links	Jerzy Zurek, GDYNIA Maritime Academy jez@kpl.pl
2.3 100GMAC 4G Core	Chris Rowen, Tensilica, rowen@tensilica.com
2.4 Artic Sand	Nadia Shalaby, MIT, nadia@sloan.mit.edu
Session 3: Security & More	Chairs Jim Simak, Sys Innovators, & Dan Hettena, Green Hills SW
8:00 PM – 10:15 PM	jsimak@systeminnovators.com danh@ghs.com
3.1 Disaster Information Computing	**J.** David Lambert, Univ. N FL, jlambert@unf.edu
3.2 Security Vision for Intel	Ernie Brickell, Intel, ernie.brickell@intel.com
3.3 Secure Distributed Computing	Mark Miller, Google, erights@google.com
3.4 **Computer Animated Films**	Gene Lee, Disney, gslee007@gmail.com

Tuesday June 28

Session 4: Consumer Electronics	Chairs Atsushi Hasegawa, Renesas, & Hirofumi Sumi, Sony
8:30 AM – 12:00 noon	atsushi.hasegawa.gx@renesas.com Hirofumi.Sumi@jp.sony.com
4.1 HS Vision Processing	Masatoshi Ishikawa, U. of Tokyo, masatoshi.ishikawa@ipc.i.u-tokyo.ac.jp
4.2 HS Switching Circuits	Bill Liu, Analog Devices Asia, bill.liu@analog.com
4.3 Ultra High Optical Network Capacity	Shu Nanmiki, Nat. Inst. Adv. Industrial Sci. & Tech., shu.namiki@aist.go.jp
4.4 4K Super-HD Video Streaming	Tatsuya Fujii, NTT Network Innovation Labs, fujii.tatsuya@lab.ntt.co.jp

Planning Session: IEEE Vail 2012, 4PM – 5:30 PM All invited to participate.

Session 5: **Potpourri**	Chairs Brian Hirano, Oracle, & Jay Fleischman, AMD
8:00 PM – 10:15 PM	brian.hirano@oracle.com jay.fleischman@amd.com
5.1 Adaptive Power Management	Mike Floyd, IBM, mfloyd@us.ibm.com
5.2 Next Gen Blue Gene	Brad McCredie, IBM, mccredie@us.ibm.com
5.3 Memristors	Steve Wald, Boise State U., swald@ieee.org
5.4 Power Management via Social Media	Steve Hammond, Lowfoot**,** shammond@lowfoot.com

Wednesday June 29

Session 6: Embedded Systems	Chairs David Baker, Green Hills SW, & Sebastien Nussbaum, AMD
8:00 AM – 12:00 noon	dbaker@ghs.com sebastien.nussbaum@amd.com
6.1 DSP Architecture	Michael Allen, Analog Devices, Michael.allen@analog.com
6.2 HEXAGON - DSP for Mobile Apps	Taylor Simpson, Qualcomm, tsimpson@quicinc.com
6.3 Ethernet Clock Synchronization	Ken Alton, Zarlink, Ken.Alton@Zarlink.Com
6.4 Embedded SW –Concept to Reality	Josef Zeevi, Jabil, Josef_zeevi@jabil.com

Arrangements Chair John M. Polhemus
John.m.polhemus@lmco.com
Committee Chair Jim Hughes
jhughes@huawei.com

General Cahir Chair Ron Bell
ron.bell@brin.com
Comm. Vice Chair Ray Barrett
raybarrett@comcast.net

Finance Chair John T. Polhemus
jtpolhemus@msn.com
Asia Pacific Chair Atsushi Hasegawa
atsushi.hasegawa.gx@renesas.com

2012 VAIL Computer Elements Workshop
June 24-27, 2012
http://projects.ccec.unf.edu/vail

New Dimensions

Program Chair: Steve Miller, NetApp, scm@netapp.com
Program Co-Chair: Yahya Sotoudeh, Intel, yahya.sotoudeh@intel.com

Sunday June 24 5 PM Registration, Dinner and Keynote Presentation (**8:00 PM – 9:15 PM)**

Next Generation

Key Note Chair: Jim Hughes, jphughes@mac.com Key Note Speaker: Jim Hughes

Monday June 25

Session 1: Internet of Things — Chairs Ray Barrett, American R & D & Mark Miller, Google,
8:30 AM – 12:00 noon — raybarrett@comcast.net erights@google.com
1. Reliability of Distributed Things — Marc Stiegler, HP Labs, erights@google.com
2. WWW Neural Network — Don Banks, Cisco, donbanks@cisco.com
3. Shipping Container Integrity Monitoring — Vipul Gupta, Oracle, vipul.x.gupta@oracle.com
4. Mobile Code on Mutually Suspicious Devices — Mark Miller, Google, erights@google.com

Session 2: I/O & Interconnect — Chairs Jim Mitchell, Oracle & Brian Hirano, Oracle
1030 pM – 4:30 PM — james.g.mitchell@oracle.com brian.hirano@oracle.com
1. Auto Commit Memory — Nisha Talagala, Fusion-IO, ntalagala@fusionio.com
2. Big Data Futures — Gaurav Makka, NetApp, gaurav.makkar@netapp.com
3. System Interconnect Innovation — Muhannad Bakir, Ga Tech, muhannas.bakir@mric.gatech.edu
4. CMOS & Si Photonics Hybrid Integration — Jack Cunningham, Oracle, john.cunningham@oracle.com

Session 3: Panel-Emerging Memory — Chairs Sam Naffziger, AMD & Steve Wald, Boise State U
8:00 PM – 10:15 PM — Samuel.naffziger@amd.com swald@ieee.org
1. In-package Memory — Pete Vogt, Intel, pete.d.vogt@intel.com

Tuesday June 26

Session 4: Consumer Electronics — Chairs Atsushi Hasegawa, Renesas, & Hirofumi Sumi, Sony
8:30 AM – 12:00 noon — atsushi.hasegawa.gx@renesas.com Hirofumi.Sumi@jp.sony.com
1. Biomed CMOS Image Sensors — Jun Ohta, NAIST, ohta@ms.naist.jp
2. FPGA Ultra Low Power — Hanpei Koike, AIST, h.koike@aist.go.jp
3. Sensor Networks — Takayuki Suyama, NTT, suyama.takayuki@lab.ntt.co.jp
4. "LTS" — Atsushi Hasegawa, Renesas, atsushi.hasegawa.gx@renesas.com

Planning Session: Vail 2013, 4PM – 5:30 PM All invited to participate.

Session 5: Panel-Medical Electronics — Chairs David Baker, Green Hills SW & Jim Simak, Harris Computer
8:00 PM – 10:15 PM — dbaker@ghs.com jsimak@harriscomputer.com
1. Electronic Stimulation Knee Rehab — Herbie Kirn, llkirn@articulatelabs.com , Articulate Labs

Wednesday June 27

Session 6: 22 nm & More — Chairs Bill Huffman, Tensilica, & Jay Fleischman, AMD
8:30 AM – 12:00 noon — huffman@tensilica.com jay.fleischman@amd.com
1. Silicon Horizons — Dinesh Somasekhar, Global Foundries, dinesh.somasekhar@globalfoundries.com
2. Embedded Multi-Core Challenges — Hang Nguyen, Intel, hang.t.nguyem@intel.com
3. TBD

Arrangements Chair John M. Polhemus
John.m.polhemus@lmco.com
Committee Chair Jim Hughes
jphughes@mac.com
Committee Vice Chair Christy She
c-she@ti.com (on leave)

Registration Chair Ron Bell
ron.bell@brin.com
Comm. Vice Chair Ray Barrett
raybarrett@comcast.net
Comm. Vice Chair Jerry Merckel
gmerckel@unf.edu

Finance Chair John T. Polhemus
jtpolhemus@msn.com
Asia Pacific Chair Atsushi Hasegawa
hasegawa.atsushi@renesas.com

2013 USENIX VAIL Computer Elements Workshop

June 23-26, 2013

Novel Computer Elements

Program Chair: Brian Hirano, Oracle, brian.hirano@oracle.com
Program Co-Chair: Steve Miller, NetApp, scm@netapp.com

Sunday June 23 5 PM Reception, Dinner and Keynote Presentation (**8:00 PM – 9:15 PM)**

Supercomputing the Universe

Key Note Speaker: Joel Primack, UCSC, joel@ucsc.edu Key Note Chair: Jim Hughes, jphughes@mac.com

Monday June 24

Session 1: Novel Processors — Chairs Yahya Sotoudeh, Intel & Pete Wilson
8:30 AM – 12:00 noon — yahya.sotoudeh@intel.com pete@kivadesigngroup.com
1.1 SeaMicro — Gary Lauterbach, AMD, gary.lauterbach@amd.com
1.2 Haswell Processesor — Rob Chappell, Intel, robert.s.chappell@intel.com
1.3 SPARC T5 — Rick Hetherington, Oracle, rick.hetherington@oracle.com
1.4 The Mill — Ivan Godard, ivan@ootbcomop.com

Session 2: **Security** — Chairs Mark Miller, Google & Dean Sutherland, CERT
1:00 PM – 4:30 PM — erights@google.com dsutherland@cert.org
2.1 Bitcoin — Brian Warner, warner@mozilla.com
2.2 Belay — Joe Politz, joe.politz@gmail.com
2.3 Tahoe-LAFS — Zooko Wilcox-O'Hearn, zooko@leastauthority.com
2.4 Thread Role Analysis for Secure Coding — Dean Sutherland, CERT, dsutherland@cert.org

Session 3: Embedded Asynchronous — Chairs Dave Baker, Firefly DSP & Marly Roncken, Portland State
8:00 PM – 10:15 PM — dave@fireflydsp.com marly.roncken@gmail.com
3.1 Multi-synchronous ICs — Ken Stevens, Granite Mountain Tech., kstevens@granitemountaintechnologies.com
3.2 Hurricane Damage Assessment — Alex Wegznek, UNF, g.wegznek@unf.edu
3.3 Asynchronous Chips for Forth Computers — Chuck Moore, GreenArrays, Inc., chipchuck@colorforth.com
3.4 Software Defined Networking — Jan Medved, Cisco, jmedved@cisco.com

Tuesday June 25

Session 4: Consumer Electronics — Chairs Atsushi Hasegawa, Renesas & Hirofumi Sumi, TSMC
8:30 AM – 12:00 noon — atsushi.hasegawa.gx@rms.renesas.com hsumi@tsmc.com
4.1 High-Speed Asynchronous Design — Makoto Ikeda, University of Tokyo, ikeda@silicon.u-tokyo.ac.jp
4.2 High-Speed vision and Manipulation — Akio Namiki, Chiba University, namiki@faculty.chiba-u.jp
4.3 Silicon Photonics and Applications — Koji Yamada, NTT Labs, yamada.koji@lab.ntt.co.jp
4.4 Augmented Service Process Reengineering — Takeshi Kurata, AIST, t.kurata@aist.go.jp

Planning Session: IEEE Vail 2014, 4PM – 5:30 PM All invited to participate.

Session 5: **Scale Out Architecture** — Chairs Michael McGrath & Don Banks, Cisco
8:00 PM – 10:15 PM — pawnmove@gmail.com donbanks@cisco.com
5.1 I/O Hinting — Mike Mesnier, Intel Research, michael.mesnier@intel.com
5.2 Implications of Next Generation Flash — Bill Moore, DSSD, bill@dssd.com
5.3 High Performance Scale Out Storage — Andy Warfield, Convergent.io, andy@convergent.io
5.4 Guaranteed QoS in the Cloud — Dave Wright, SolidFire, wrightd@gmail.com

Wednesday June 26

Session 6: Novel Materials — Jim Hughes, Seagate
8:30 AM – 12:00 noon — jphughes@mac.com
6.1 Hydrogen Depassivation Lithography — Josh Ballard, Zyvexlabs, jballard@zyvexlabs.com
6.2 Edison Returns! — Ron Vinsant, Exar, ron@poweracumen.com
6.3 Future of Tape — Richard Dee, Quantum, richarddee@comcast.net
6.**4 Future of Rotating Storage** — Tim Rausch, Seagate, tim.rausch@seagate.com

Committee

Arrangements Chair	John M. Polhemus	john.m.polhemus@lmco.com
General Chair	Ron Bell	rkbell0@comcast.net
Finance Chair	John T. Polhemus	jtpolhemus@msn.com
Committee Chair	Jim Hughes	jphughes@mac.com
Committee Vice Chair	Ray Barrett	raybarrett@comcast.net
Asia Pacific Chair	Atsushi Hasegawa	atsushi.hasegawa.gx@rms.renesas.com
Committee Chair Emeritus	Gerald Merckel	gmerckel@unf.edu

USENIX The Advanced Computing Systems Association

2014 VAIL Computer Elements Workshop

June 22-25, 2014

Theme: Possible Futures

Sunday June 22nd 5 PM Registration and Dinner. Keynote Presentation (8:00 PM – 9:15 PM)
Key Note Speaker: Robin Hanson (George Mason University) rhanson@gmu.edu

Keynote: Prediction Markets Giving the Truth Orientation of Engineers to Everyone Else

Program Chair: Mark S. Miller (Google) erights@google.com
Program Co-Chair: Brian Hirano (Oracle) brian.hirano@oracle.com
Key Note Chair: Jim Hughes (Seagate) jphughes@mac.com

Monday June 23rd

Session 1: **Security**	Chairs: Joe Politz (Brown Univ), Dean Sutherland (CERT)
9:00 AM – 12:00 noon	joe.politz@gmail.com, dfsuther@cs.cmu.edu
Securing Software Defined Networks	Arjun Guha (UMass Amherst) arjun@cs.umass.edu
Shill (Caps-based Scripting)	Scott Moore (Harvard) sdmoore@fas.harvard.edu
Secure Coding	Daniel Plakosh (CERT) dplakosh@cert.org
Session 2: **Concurrency in Prog. Languages**	Chairs: Brian Hirano (Oracle), Jan Medved (Cisco)
1:00 PM – 3:30 PM	brian.hirano@oracle.com, jmedved@cisco.com
EM2 Scalable Multicore Architecture	Mieszko Lis (MIT) mieszko@csail.mit.edu
Harnessing Hardware Parallelism with Erlang	Jim Larson (Google) jimlarson@google.com
Resilient & Petascale X10	David Cunningham (Google) sparkprime@gmail.com
Session 3: **Imaging and Signal Processing**	Chairs: Hirofumu Sumi (TSMC), Makoto Ikeda (Univ. of Tokyo)
3:40 PM – 4:30 PM	hsumi@tsmc.com, ikeda@silicon.u-tokyo.ac.jp
Full-spec UHDTV-2 Video System	Hiroshi Shimamoto (NHK) shimamoto.h-iu@nhk.or.jp
7:30 PM – 10:30 PM	
Imaging Technologies	Eric Fossum (Dartmouth College) Eric.R.Fossum@dartmouth.edu
Highlights of the Imaging World	Boyd Fowler (Google) boydfowler@google.com
3D CMOS Image Sensors and System	Masayuki Shimura (Sony) Masayuki.Shimura@jp.sony.com
	Hirofumu Sumi (TSMC), Makoto Ikeda (U. Tokyo)
Panel Discussion	All

Tuesday June 24th

Session 4: **Wireless and Networking**	Chairs: Ed Callaway (Sunrise Micro Devices), Don Banks (Cisco)
9:00 AM – 12:00 noon	ed@sunrisemicro.com, donbanks@cisco.com
Wireless IP and Embedded MCUs	David Flynn (ARM) David.Flynn@arm.com
Network-Centric Programming Languages	Jon Rossie (Cisco) jorossie@cisco.com
Scaling High Performance Managed Clusters	Landon Noll (Cisco) chongo@cisco.com

Planning Session: IEEE Vail 2015, 4PM – 5:30 PM All invited to participate.

Session 5: **Consumer Electronics**	Chairs: Atsushi Hasegawa (Renesas), Yoshio Masubuchi (Toshiba)
8:00 PM – 10:30 PM	atsushi.hasegawa.gx@renesas.com, yoshio.masubuchi@toshiba.co.jp
Surprise LCD Uses: 3D Vision & G-Sync	Gerrit Slavenburg (NVIDIA) gslavenburg@nvidia.com
A Novel Power Play for Distributed LEDs	Tsutomu Shimomura (Neofocal Systems) tsutomu@neofocal.com
Energy Efficient Many-Core SoC	Hiroyuki Usui (Toshiba) hiroyuki1.usui@toshiba.co.jp

Wednesday June 25th

Session 6: **Processors**	Chairs: Yahya Sotoudeh (Intel), Pete Wilson (Freescale)
9:00 AM – 12:00 noon	yahya.sotoudeh@intel.com, pete@kivadesigngroup.com
Heterogeneous Computing and its Low Power Considerations	
	Roy Ju (Mediatek) roy.ju@mediatek.com
Xbox One: Next Gen Game Processor	Sebastien Nussbaum (AMD) sebastien.nussbaum@amd.com
	John Sell (Microsoft) jsell@microsoft.com
Freescale's Advanced IO Processor	Brian Kahne (Freescale) bkahne@freescale.com

Local Arrangements, VCEW Support	General Chair Ron Bell	Committee Chair Jim Hughes
john.m.polhemus@lmco.com	ron.bell@brin.com	jphughes@mac.com
Committee Vice Chair Ray Barrett	Asia Pacific Chair Atsushi Hasegawa	Committee Chair Emeritus Gerald Merckel
raybarrett@comcast.net	atsushi.hasegawa.gx@renesas.com	gmerckel@unf.edu

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2015 USENIX VAIL Computer Elements Workshop

June 28-July 1, 2015

The Evolving Data Center

Program Chair: Steve Miller, Intel, steven.c.miller@intel.com

Sunday June 28 5 PM Registration, Dinner and Keynote Presentation (8:00 PM – 9:15 PM)

Security Post Snowden

John Callas, Co-founder & CTO Silent Circle

Key Note Chair: James Hughes, jphughes@mac.com

Monday June 29

Session 1: Machine Learning — **Chairs: David Cunningham & Sebastien Nussbaum**
8:30 AM – 12:00 noon — sparkprime@gmail.com Sebastien.Nussbaum@amd.com

1. Integrating living cells with CMOS — Hua Wang, Georgia Inst of Tech, hua.wang@ece.gatech.edu
2. Stoke: A stochastic optimizer for the x86_64 — Eric Schkufza, Stanford University, eschkufz@cs.stanford.edu
3. Quantum Computing on classical computer — Arun Majumdar, Kyndi, arun@kyndi.com
4. Weaver, a self timed testable crossbar — Ivan Sutherland, Portland State, ivans@cecs.pdx.edu

Session 2: Processor Technology — **Chairs: Pete Wilson & David Flynn**
1:30 PM – 4:30 PM — pete@kivadesigngroupe.com david.flynn@arm.com

1. Cavium Thunder X — Shubu Mukherjee, Cavium, shubu.mukherjee@cavium.com
2. CHERI a capability system — Robert Watson, Cambridge, robert.watson@cl.cam.ac.uk
3. Introduction to ARM version 8 — Richard Grisenthwaite, ARM, Richard.Grisenthwaite@arm.com
4. Quarq efficient architecture for embedded — Brian Kahne, Freescale, bkahne@freescale.com

Session 3: Capability Systems — **Chairs: Scott Moore & Dean Sutherland**
8:00 PM – 10:15 PM — sdmoore@fas.harvard.edu dfsuther@cs.cmu.edu

1. seL4/L4 — Gernot Heiser, NICTA, gernot@nicta.cam.au
2. Nested Kernel: OS Arch for Intra-Kernel — Nathan Dautenhahn, UIUC, dautenh1@illinois.edu
3. A Blessing-Based Authorization Model — Ankur Taly, Google, ataly@google.com

Tuesday June 30

Session 4: Storage Class Memory — **Chairs: Jay Fleischman & Yahya Sotoudeh**
8:30 AM – 12:00 noon — Jay.Fleischman@amd.com yahya.oitoudeh@intel.com

1. Storage for Virtualized Workloads — Jim Pinkerton, Microsoft, jpink@microsoft.com
2. Roadmap and Interface Challenges for SCM — Mike Ignatowski, AMD, Mike.Ignatowski@amd.com
3. Memory at the end of the Roadmap — Gary Bronner, Rambus, gbronner@rambus.com
4. Benefits of emerging memory tech — Foltin Martin, HP, martin.foltin@hp.com

Planning Session: Vail 2016, 4PM – 5:30 PM All invited to participate.

Session 5: Consumer Technology — **Chairs: Atsushi Hasegawa & Yoshio Masubuchi**
8:00 PM – 10:15 PM — atsushi.hasegawa.gx@renesas.com yoshio.masubuchi@toshiba.com.jp

1. SoCs for Industrial and factory automation — Atsushi Hasegawa, atsushi.hasegawa.gx@renesas.com
2. SoC for ADAS — Toru Sano, Toshiba, toru.sano@toshiba.co.jp
3. 8K DTV Technology — Mitsuo Ikeda, NTT,ikeda.mitsuo@lab.ntt.co.jp

Wednesday July 1

Session 6: Big Data — **Chairs: Jim Larson & James Hughes**
8:30 AM – 12:00 noon — jimlarson@google.com james.hughes@seagate.com

1. Trends in Datacenter Architectures — Mike McGrath, Intel, Michael.mcgrath@intel.com
2. Key Value Store Hard Drive — James Hughes, Seagate james.hughes@seagate.com
3. Yedalog: Exploring Knowledge at Scale — Mark Miller, Google erights@google.com
4. JSonnet, Terraform & Packer — Dave Cunningham, Google dcunnin@google.com

Committee Chair	James Hughes	jphughes@mac.com
Asia Pacific Chair	Atsushi Hasegawa	hasegawa.atsushi@renesas.com
Local Arrangements	VCSW Support Corp	jpbookworm23@gmail.com

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2016 USENIX
VAIL Compute[illegible] Elements Workshop
June 19 -June 22, 2016

Program Chair: David Flynn, ARM, david.Flynn@arm.com
Program Co Chair: Steve Miller, Intel, steven.c.miller@intel.com

Sunday June 19, 5 PM Registration, Dinner and Keynote Presentation

Cryptography in the New World Order
John Kelsey, NIST

Key Note Chair: Jim Hughes, jphughes@mac.com

Monday June 20
9:00 AM – 12:00 noon
Session 1: Processors Chairs: Jay, Fleischman, AMD, Jay.Fleischman@amd.com
Richard Grisenthwaite, ARM, richard.Grisenthwaite@arm.com

- **Intel Quark Processor** Venkat Madduri, Intel, venkateswara.madduri@intel.com
- **RISC-V: Instruction sets want to be free** Krste Asanovic, UC Berkeley, krste@berkeley.edu
- **X-Gene3** Greg Favor, AppliedMicro, gfavor@apm.com

1:30 PM – 4:30 PM
Session 2: Consumer Chairs: Atsushi Hasegawa, Renesas, atsushi.hasegawa.gx@renesas.com
Yoshio Masubuchi, Toshiba, yoshio.masubuchi@toshiba.co.jp

- **Normally-Off Computing** Hiroshi Nakamura, Univ Tokyo, nakamura@hal.ipc.i.u-tokyo.ac.jp
- **Microcontroller for Small Sensing Nodes** Masami Nakajima, Renesas, masami.nakajima.wj@renesas.com
- **LIDAR for ADAS and autonomous vehicles** Ken Tanabe, Toshiba, kenn.tanabe@toshiba.co.jp
- **Automotive Lidar technologies** Harvey Weinberg, Analog Devices, harvey.weinberg@analog.com

Tuesday June 21
9:00 AM – 12:00 noon
Session 4: OS and Security Chairs: Michael Allen, Analog Devices, michael.allen@analog.com
Steve Miller, Intel, steven.c.miller@intel.com

- **Barrelfish: an operating system for modern hardware** Timothy Roscoe, ETH, troscoe@inf.ethz.ch
- **SeaOS: A simple OS for multicore Machines** Daniel Bittman, UCSC, danielbittman1@gmail.com
- **Haven: Shielding Applications from an Untrusted Cloud** Andrew Baumann, Microsoft, Andrew.Baumann@microsoft.com
- **Failure Provenance Analysis: From Crashdump to Shellcode**
  Parker Thompson, Leviathan, Parker.Thompson@leviathansecurity.com
  Baron Von Oldenberg, Baron.Oldenburg@leviathansecurity.com

Planning Session: VCEW 2017, 4PM – 5:30 PM All invited to participate.

8:30 PM – 10:00 PM
Session 5: Internet of Things Chairs: Pete Wilson, NXP, peter.wilson@nxp.com
Bill Huffman, Cadence (Tensilica), huffman@alum.mit.edu

- **IoT: The Next Technology Cycle** Krisztian, Flautner, ARM, Krisztian.Flautner@arm.com
- **Bringing Deep Learning to the Mass Market** Samer Hijazim, Cadence, shijazi@cadence.com

Wednesday June 22
9:00 AM – 12:00 noon
Session 6: Process and GPU Chairs: Yahya Sotoudeh, Intel, yahya.sotoudeh@intel.com
David Flynn, ARM, david.Flynn@arm.com

- **Low Voltage SRAM** David Burnett, Global Foundries, david.burnett@globalfoundries.com
- **Accelerating Hyper Cloud Data Center Solutions with Breakthrough Integration Technologies**
  Sanjay Charagulla, Global Foundries, sanjay.charagulla@globalfoundries.com
- **The Bifrost GPU architecture and the ARM Mali-G71 GPU** Jem Davies, ARM, Jem.Davies@arm.com

VCEW Support Corp: John M. Polhemous
jpbookworm23@gmail.com
Committee Chair: Jim Hughes
jphughes@mac.com

Registration Chair: Jim Hughes
jphughes@mac.com
Comm. Vice Chair: Steve Miller
steven.c.miller@intel.com

Finance Chair:
TBD
Asia Pacific Chair: Atsushi Hasegawa
hasegawa.atsushi@renesas.com

2017 USENIX Vail Computer Elements Workshop

The USENIX Vail Computer Elements Workshop is a unique four day workshop that has been around for 47 years serving leading architects of the computer industry. This intentionally small workshop is intended to allow a lively interaction between the participants and the speakers. The agenda is 100% invited technical talks and the audience is mostly previous speakers. Past keynotes have been Seymour Cray, Gordon Moore, Burton Smith, and Ivan Sutherland.

The workshop will be held June 18 - 21, 2017 at the Christiania at Vail.

Keynote

This year's Keynote will be ***Rebuilding the Cambridge EDSAC*** by Andrew Herbert

Bio

Herbert received his Ph.D. in Computer Science from Cambridge University in 1978 for his work on "A Microprogrammed Operating System Kernel" and worked with Maurice Wilkes and Roger Needham and others on the "Cambridge Model Distributed System". Later he joined Microsoft Research Cambridge as managing director and chairman of Microsoft Research EMEA. Herbert was appointed Officer of the Order of the British Empire (OBE) in the 2010 New Year Honours, and is a Fellow of the Royal Academy of Engineering. Now in retirement, Herbert is the director of a project to construct a working replica of the Cambridge EDSAC computer.

Registration is open here.

Preliminary Program

Next generation Atom core	Intel
Nervana - Deep Learning processor	Intel
Nano-Engineered Computing Systems Technology, or N3XT	Stanford
IBM Power9	IBM
OpenCAPI	IBM
Ryzen - AMD's new core	AMD
Intel's 3DNAND and 3DXP storage class products	Intel
Persistent Memory: The Benefits and the Challenges	Intel
The Next Step in Computing: Neuromemristive Processors	Knowm Inc
Evolutionary advances in memory, Revolutionary implications for applications	Sandisk
Motor Control for next generation HEV/EV	Renesas
4k/8k TV Solution	Socionext
Time Domain Neural Network	Toshiba
Movidius	Intel
Machine vision on a chip: non-mechanical laser radar enabled by liquid crystal waveguides	Analog Devices
Of categories and computers: a story unfolding	Tim Carstens
Scale out object storage	Keeper Technology
Practical Quantum Computing and the Rigetti Quantum Computer	Rigetti Quantum Computing
Reading Tea Leaves: Extrapolating meaning from plaintext size of encrypted blobs	Josh Pitts
Cassandra, Scale out database	Apple
Artificial Intelligence & Machine Learning: Entrepreurship & Technology Buildouts	CDL
Tensorflow	Google
Exa-scale IOT Network Designs for Machine Learning and Big Data	Kyndi, Inc

Program Committee

Chair: Bill Huffman Cadence (Tensilica)
Co-Chair: David Flynn, ARM
Yahya Sotoudeh, Intel
Jay Fleischman, AMD
Steve Miller, Intel
Pete Wilson, Kiva Design Groupe
Atsushi Hasegawa, Renesas
Yoshio Masubuchi, Toshiba
Jem Davies, ARM
Michael Allen, Analog Devices
Parker Thompson, Leviathan
Baron Von Oldenberg, Leviathan
Arun Majumdar, Kyndi, Inc
Richard Grisenthwaite, ARM

Venue

The workshop is "all inclusive". The workshop fee covers the event, housing and all food from dinner Sunday through lunch Wednesday.

Fees will be:

	Early	Late after June 1
Usenix Members	$995	$1095
Non-members	$1095	$1195

Registration

Registration fees include the workshop, lodging and meals. The prices increase by $100 on June 5th.

- Extra days can be purchased for $180.
- Companions are welcome and their fee is $495 and includes all meals and receptions.
- Detailed receipts will be provided at the workshop for those who need them. Paying at the workshop is possible.
- Cancellation is possible before June 9th.
- For more information please contact James Hughes.

Sponsored by the Vail Computer Elements Workshop in cooperation with

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Vail Computer Elements Workshop 2018

Sunday, June 24, 2018

5:00-6:30 pm Social Hour: **AD-4 Condo** (Directions available at the Christiania Hotel)

6:30- 8:00 pm **Dinner** **Restaurant: Left Bank** *(substitute for the closed Campo Di Fiore)*

8:00-9:30 pm **Keynote:** **Speed doesn't matter if you can't drive it,** *Stephanie Rosenbaum, TecEd, Inc.*

Monday, June 25, 2018

7:30-9:00 am Breakfast: Sarah's Lounge

9.00am *Opening Words - Jim Hughes*

Session 1 Consumer Electronics

Chairs: *Atsushi Hasegawa, Renesas; Yoshio Masubuchi, Toshiba Memory*

9:00-9:45 am	1.	Endpoint AI Chip,	*Atsushi Hasegawa, Renesas*
9:45- 10:30 am	2	Near-Data Computing,	*Jun Deguchi, Toshiba Memory*
10:30-10:45 am		*Break & Group Picture*	
10:45-11:30 am	3	MPEG Media Transport Technologies and its application to immersive media communication services ,	*Takayuki Nakachi, NTT*
11:30 -12:15 pm	4	Side Channel Attacks in the Real World	*Bot, Ordo Labs*

12:15-1:30 pm Lunch: Sarah's Lounge

Session 2 Processors

Chairs: *Yahya Sotoudeh Intel; Steve Miller Intel*

1:30-2:15 pm	1	Cavium ThunderX2 Processor	*Rabin Sugumar, Cavium*
2:15-3:00 pm	2	RISC-V FireSim/FireBox	*Sagar Karandikar, UC Berkeley ADEPT Lab*
3:00 -3:15 pm		*Break*	
3:15-4:00 pm	3.	ARM Machine Learning Processor	*Ian Bratt, ARM*
4:00-4:45 pm	4.	AMD EPYC	*Jay Fleischman, amD*

4:45-5:00 pm *Break*

5:00-6:15 pm **Social Hour:** **AD-4 Condo**

6:15-8:00 pm **Dinner** **Restaurant: The Lancelot**

Session 3

8:00-9:30 pm 1 From Exabytes to Nobel Prizes *Fons Rademakers, CERN*

Tuesday, June 26, 2018

7:00-8:30 am Breakfast: Sarah's Lounge

8:30 am **Session 4 Database + Processors**
Chairs: *Pankaj Mehra, Samsung, Arun Majumdar, Kyndi, Inc*

8:30-9:15 am	1	Systems and Machine Learning	*Amir Khorsrowshahi, Intel (Nervana)*
9:15-10:00 am	2	BigStream	*Maysam Lavasani, BigStream*
		10:00 am 10:15 am Break	
10:15-11:00 am	3	Massive Shared Memory on Commodity Processors	*Steffan Persvold, Numascale*
11:00-11:45 am	4	3DIC	*Don Draper, ProPrincipia*

11:45-1:00 pm Lunch Sarah's Lounge

1:00-4:00 pm *Afternoon Free*

4:00-5:00 pm Planning Meeting in Sara's Lounge
Optional, but please attend to help plan VCEW 2019
Refreshments provided

5:00-6:00 pm **Social Hour:** **AD-4 Condo**

6:00-8:00 pm **Dinner Restaurant: Left Bank**

Session 5 Accelerators
Chairs: *Mike Nelson, Intel; Steve Fields, IBM*

8:00-8:45 pm	1	Microsoft Brainwave: Flexible Deep-Learning Accelerator	*Eric Chung, Microsoft* Research
8:45-9:30 pm	2	Intel's Acceleration Stack Tool Chain for Xeon CPUs with FPGAs	*Michal Skiba, Intel (PSG)*

Wednesday, June 27, 2018

7:00-8:30 am Breakfast: Sarah's Lounge

Session 6 Programming Languages + Internet Economy
Chairs: *Andy Rudoff, Intel; Pete Wilson, Kiva Design Groupe; Rich Zippel , Google; John Kelsey, NIST*

8:30-9:15 am	1	Computer Architecture Considered Harmful	*Pete Wilson Kiva Design Groupe*
9:15-10:00 am	2	Marketing for the 21st Century: Online Behavioral and Contextual Ads	*George Salem*
		10:00-10:15 am Break	
10:15-11:00 am	3	Enhancing Java for Persistent Memory	*Steve Dohrmann Intel*
11:00-11:45 am	4	The NIST Beacon and Public Randomness	*John Kelsey NIST*

11.45 *Closing words - Jim Hughes.*

11:45-1:00 pm *Lunch*

2019 Vail Computer Elements Workshop

JUNE 23-JUNE 26, 2019 AT THE CHRISTIANIA, VAIL

Program Chair: **Steve Miller, Intel**
Program Co-Chair: **Brian Hirano, Oracle**

Sponsored by the Vail Computer Elements Workshop in cooperation with

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Photographed at the Inmos factory, Newport, Wales.
https://www.sciencephoto.com/media/76521/view/iann-barron-electronics-engineer

Keynote: Back to the Future- *Iann M Barron*

Iann Marchant Barron CBE is a British computer engineer and entrepreneur, born in June 1936.

During vacation work in 1956-7 at Elliott Brothers while still at Cambridge he designed the Elliott 803.[1] On leaving University he joined the Civil Service in 1958 as a Scientific Officer on special assignment first to the Army Operational Research Group, and in 1960 to the Air Ministry.

He returned to the company now called Elliott Automation as a Project Leader for the Elliott 502 computer team, later becoming the company's Head of System Research.

In 1965 Barron left Elliott Automation to become Founder and Managing Director of Computer Technology Limited, where the Modular One range of computer systems was developed.

In the mid-1970s he formed a new company, Microcomputer Analysis Ltd, which offered consultancy on microprocessors to the semiconductor industry. This brought him into contact with two eminent American semiconductor specialists, Richard Petritz and Paul Schroeder, and in 1978 the triumvirate founded Inmos International PLC, which produced the innovative transputer, and led to the development of SpaceWire.

Barron was elected a Distinguished Fellow of the British Computer Society (DFBCS) in 1986 and was appointed CBE in the 1994 New Year Honours.

Sunday June 23

5.00 pm *Registration*
5.00 pm *Reception*
6.30 pm *Dinner at La Nonna restaurant*

8.30 pm **Keynote: Back to the Future**- *Iann M Barron*

Monday June 24

8.00 am *Self-service breakfast in Sarah's Bar, Christiania*

9.00 am-12 noon **Session 1 - Processors**

Chairs: Yahya Sotoudeh, Intel

1. IBM Power processor and Future Trends - *Edmund Gieske, IBM*
2. Vega 20: World's First 7nm GPU, with 25Gb/s links &1 TB/sec Memory BW - *Sam Naffziger, AMD*
3. *Group Picture*
4. Energy-Efficient Design Using Sparsity & Low Precision for Edge Computer - *Cormac Brick, David Bernard, Intel*
5. ARM Helium - *Tom Grocutt, ARM*

12 noon *Lunch in Sarah's Bar, Christiania*

1.30 pm - 4.30 pm **Session 2 - Processors & Consumer Electronics**

Chairs: Atsushi Hasegawa, Renesas; Yoshio Masubuchi, Toshiba Memory Corp

1. ARM-SVE enabled post-K processor for energy efficiency and sustained application performance in HPC - *Mitsuhisu Sato, Riken and Toro Shimizu Tokyo University*
2. Multicore SoC with DNN Acceleration for Automotive Applications - *Masato Uchiyama, Toshiba Device & Storage*
3. Automotive Flash Microcontroller with Virtualization-Assisted Processor - *Sugako Otani, Renesas Electronics*
4. Storage Economics: The Value in Storing the Long Tail - *James Hughes, UCSC*

5.00 pm *Reception*

6.30 pm *Dinner at the Lancelot Restaurant*

Tuesday June 25

8.00 am *Self-service breakfast in Sarah's Bar, Christiania*

9.00 am-12 noon **Session 4 - Sensors, IoT, 5G, Automotive and Security**

Chairs: Michael Allen, ARM; Pete Wilson, Kiva Design Groupe; b0t, Ordo Labs; Bill Huffman, Cadence/ Tensilica

1. Photonics: a Bright Legacy and Future - *Derek Gann, Analog Devices, Inc*
2. Secure Machine Learning at the Edge - *Rob Oshana, NXP*
3. Hacking Telephony 1970 style - *Bill Soley, BillTech*
4. Automotive Control Systems Security - *Peter Gutman, University of Auckland*

12 noon *Lunch in Sarah's Bar, Christiania*

1.30 pm - 4.00 pm: Free time to explore and socialize

4.00 pm Planning Session for VCEW 2020. All invited. In Sarah's Bar, Christiania

5.00 pm *Reception*
6.30 pm *Dinner at the Left Bank Restaurant*

8.30 pm - 10.00 pm **Session 5 - Programming Languages**

Chairs: Ian Bratt, ARM; Gary Lauterbrach, Cerebras

1. Programming Persistent Memory with golang - *Pratap Subrahmanyam, VMWare*
2. Using persistent object memory for dataflow computing - *Ethan Miller, UCSC*

Wednesday June 26

8.00 am *Self-service breakfast in Sarah's Bar, Christiania*

9.00 am-12 noon **Session 6 - AI/ML and Data**

1. The Cerebras CS-1 AI Accelerator - *Sean Lie, Cerebras*
2. Xilinx Versal AI Engine - *Samuel Bayliss, Xilinx*
3. Architecting Nvidia GPUs for Deep Learning performance - *Ronny Krashinsky, Nvidia*
4. Beyond CMOS for AI - *Amir Khosrowshahi, Intel*

12 noon *Packed Lunch in Sarah's Bar, Christiania*

Close.

The Prize for the Best Talk at VCEW 2019 was awarded to Sean Lie of Cerebras.

Sponsored by the Vail Computer Elements Workshop in cooperation with

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Virtual VCEW 2020 Program

June 20-23, 2020

Program Chair: Don Soltis, Intel
Program Co-Chair: Steve Miller, Intel

Monday June 22

8:30 pm **Keynote: Whitfield Diffie**: The Lessons of 20th Century Cryptography Processors

Bailey Whitfield 'Whit' Diffie is an American cryptographer and one of the pioneers of public-key cryptography along with Martin Hellman and Ralph Merkle. Diffie and Hellman's 1976 paper New Directions in Cryptography introduced a radically new method of distributing cryptographic keys, that helped solve key distribution—a fundamental problem in cryptography.

Processors – Chair: Edmund Gieske, IBM

9:00 am IBM Z15 – **Christian Jacobi**, IBM
10:00 am Samsung M5/6 – **Brian Grayson**, formerly Samsung
11:00 am Breakout rooms for networking
12:00 pm Break

Security – Chair: John Kelsey, NIST

1:00 pm RISC V security architecture – **Helena Handschuh**, Cryptography Research
2:00 pm The NIST lightweight crypto competition – **Kerry McKay**, NIST

Consumer Electronics – Chair: Yoshio Masubuchi

3:00 pm Accelerating neuroscience data processing with high-speed storage – **Yosuke Brando**, Kioxia

Tuesday June 23

IO Interconnect – Chair: Yahya Sotoudeh, Intel

8:00 am	TeraPHY: High density Electronic-Photonic Chiplet for optical I/O from a Multichip module – **Mark Wade,** Ayar Labs
9:00 am	CCIX Cache Coherent Interconnect for Emerging acceleration application – **Mittal** , Xilinx
10:00 am	OpenCAPI 4.0 – **Jeff Stuecheli**, IBM
11:00 am	Breakout rooms for networking
12:00 pm	Break

Software – Chair: Brian Hirano, Bigstream

1:00 pm	TVM: An Automated End-to-End Optimizing Compiler for Deep Learning – **Tianqi Chen**, CTO of OctoML
2:00 pm	ML Benchmarking – **Gennady Pekhimenko**, University of Toronto

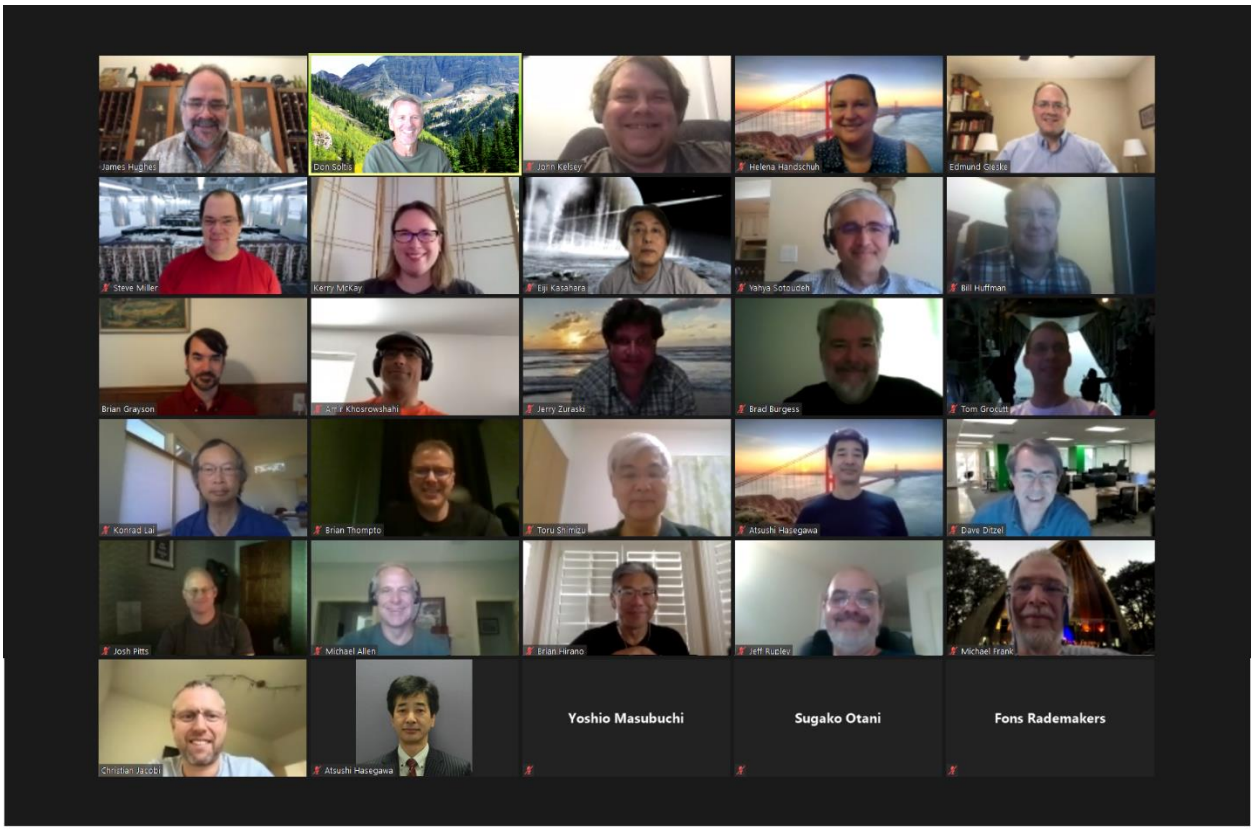
Memory – Chair: Michael Allen, ARM

3:00 pm	Hybrid Memory – **Damir Jamsek**, IBM

VCEW 2020 Best Talk Award

Congratulations Mark Wade!

VCEW 2020 Photo



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VCEW 2021 Program

June 20-23, 2021 Virtual and the Christiania, Vail

Program Chair: Don Soltis, Intel
Program Co-Chair: Brian Hirano, Micron

Sunday June 20

All times are in Mountain Daylight TZ

5:00 pm Local attendees: Registration and Reception TBA
6:30 pm Local attendees: Dinner TBA
8:30 pm **Keynote: Robert Hormuth, AMD**

Abstract: In the Future 4 Worlds of the IT industry there are 2 major unknown questions that could shape the landscape for technology, innovation, and the market for decades to come. In this talk we will explore 4 possible worlds of the future; how we would get there, how the players will react, and who wins and loses in each outcome.

Monday June 21

8:00 am Local attendees: Breakfast
9:00 am **Welcome** Join

Session 1 **Processors – Chair: Edmund Gieske**
9:15 am *Cezanne APU*, Sonu Arora, AMD
9:45 am *GPU*, Mike Mantor, AMD
10:15 am TBA
10:45 am TBA

Breakout

11:30 am	Processors	Processors Breakout Link
	Consumer Electronics	Consumer Electronics Breakout Link
	I/O Interconnect	I/O Interconnect Breakout Link
	Security	Security Breakout Link
	Software	Software Breakout Link
	Memory	Memory Breakout Link

12:00 pm Lunch

Session 2 **I/O Interconnect – Chair: Yahya Sotoudeh, Intel**
1:30 pm *CXL*, Debendra Das Sharma, Intel
2:00 pm *Luminous Si-Photonics*, Dave Baker
2:30 pm TBA

Consumer Electronics – Chair: Yoshio Masubuchi, Kioxia
3:00 pm *Fugaku Supercomputer*, Dr. Matsuhisa Sato, Riken

5:00 pm Local attendees: Reception
6:30 pm Local attendees: Dinner at Lancelot

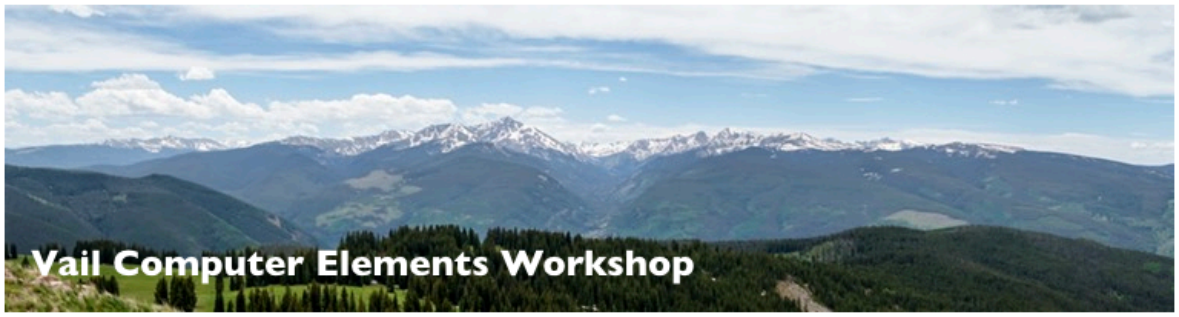
Tuesday June 22

8:00 am	Breakfast	
Session 3	**Memory – Chair: Michael Allen, ARM**	
9:00 am	*Architecture Support for Persistent Storage*, William Wang, ARM	
9:30 am	*LPDDR5 Functional Safety*, Stephen Buch, Micron	
	Security – Chair: Amy Santoni, Intel	
10:00 am	*Post-Quantum Cryptography Competition*, Dustin Moody, NIST	
10:30 am	*Fully Homomorphic Encryption Work with DARPA*, Rosario Cammarota, Intel	
11:00 am	TBA	
	Breakout Session	
11:30 am	Processors	Processors Breakout Link
	Consumer Electronics	Consumer Electronics Breakout Link
	I/O Interconnect	I/O Interconnect Breakout Link
	Security	Security Breakout Link
	Software	Software Breakout Link
	Memory	Memory Breakout Link
12:00 pm	Lunch	
1:30 pm – 4:30 pm	Free time to enjoy Vail	
4:00 pm	Planning session for VCEW 2022	
5:00 pm	Local attendees: Reception	
6:30 pm	Local attendees: Dinner at Left Bank	

Wednesday June 23

8:00 am	Breakfast
Session 4	**Software - Chair: Brian Hirano, Micron**
9:00 am	*Personal Recommendation Systems*, Sean (Hsien-Hsin) Lee, Facebook
9:30 am	*MLCommons*, David Kanter, MLCommons
10:30 am	*Protocol/Flat Buffers – Low Latency/Efficient Data Transport*, Brian Hirano, Micron
11:00 am	*MemVerge (Memory Virtualization)*, Charles Fan, MemVerge
11:30 am	*"Glitch" Programming*, David Hulton, Micron

Close



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VCEW 2023 Program

All Times Mountain Daylight Time (UTC-6)

Program Chair: Rich Zippel, Google
Program Co-Chair: Brian Hirano, Micron

Sunday June 11

5:00 pm Local attendees: Registration and informal gathering
6:30 pm Dinner: Left Bank
8:30 pm **Keynote:** *Verifiable Election Technologies: Enabling Voters to Confirm that their Votes are Accurately Counted* — Josh Benaloh, Microsoft

Monday June 12

7:30 am Continental Breakfast: The Lodge at Vail
8:30 am *Welcome*: Jim Hughes, Apple, VCEW Executive Committee Chair

Session 1 Processors
8:45 am *Challenges of Designing Processors given Data Center Power Constraints*, Ryan Tabrah, Intel
9:30 am *The Parameter and Chip Wars: Moving Beyond Model-Centric AI to Sustainable Data-centric AI for Systems*, Vijay Reddi, Harvard University
10:15 am *15-Minute Break*

10:30 am *DRAM at the End of Moore's Law: Device and System Implications*, Thomas Vogelsang, Rambus
11:15 am *Memory-Semantic SSD™: CXL-Era Memory Expansion with DRAM and NAND Flash Media*, Rekha Pitchumani, Samsung
12:00 pm Lunch: The Lodge at Vail

Session 2 Software
1:30 pm **Server Telemetry – Expanding the Horizon Beyond Code Optimization (by video)*, Corey Gough, Intel
2:15 pm **Computation Energy Efficiency – present and future (by video)*, Efi Rotem, Intel
3:00 pm 15-Minute Break
3:15 pm *Revisiting Server Memory Architectures*, Chris Peterson, Meta
4:00 pm **System Foundations for Disaggregated Memory (by video)*, Pankaj Mehra, Elephance Memory
5:00 pm Reception in Vail Village
6:30 pm Dinner: La Nonna

Panel Session Compute Express Link (CXL)
8:30 pm *Participants to be decided*

Tuesday June 13

7:30 am Continental Breakfast: The Lodge at Vail

Session 3 Security
8:45 am *Compromising cryptographic keys through spontaneous faults in the wild*, Nadia Heninger, UCSD
9:30 am *TBD*, Josh Hill, KeyPair Consulting
10:15 am Capability Security, Cambridge CHERI and ASU BGAS. Andy "Cap" Glew

11:00 am 15-minute BreakSession 4 Consumer Electronics
11:15 am *QC-HPC hybrid computing for simulation & data-analysis hybrid applications*, Hiroaki Kobayashi, Tohoku University
12:00 pm Lunch: The Lodge at Vail

1:30 pm – 4:00 pm **Free time to enjoy Vail**

4:00 pm Planning session for VCEW 2024
5:00 pm Reception
6:30 pm Dinner: Lancelot

Wednesday June 14

7:30 am Continental Breakfast: The Lodge at Vail
Grab and go lunches will be available starting at 10:30

Session 5 HPC

8:45 am **RISC V in an HPC World (by video)*, Charlie Cheng, Andes Technology
9:15 am Apollo M/L Super Computer, David Baker, Luminous Computing

10:00 am *15-Minute Break*

Session 6 Quantum

10:15 am *Quantum-centric supercomputer-speed, quality and scale*, Andrew Wack, IBM
11:00 am *Quantum Compilers*, Thomas Alexander, IBM
11:45 pm *Final Thoughts*: Jim Hughes

Program brought to you by your VCEW 2023 Session Chairs

Processors: Yahya Sotoudeh, Intel and Edmund Gieske, Micron
Consumer Electronics: Atsushi Hasegawa, University of Tokyo and Yoshio Masubuchi, Kioxia
Quantum: Andrew Wack, IBM and Antia Lamas-Linares, Amazon
Security: Amy Santoni, Intel and John Kelsey, NIST
Software: Rajshree Chabukswar, Intel and Brian Hirano, Micron
HPC: Pete Wilson, BSC and David Baker, Luminous Computing